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Original scientific paper

Design and Optimization of a CMOS Inverter-Based Low-Noise Amplifier for Enhanced Gain and Efficiency in Wearable Electronics

SHOBANA NAGESWARI C.*, SETU GARG, RADWA MARZOUK, SHAHUL HAMEED SHABEER S.

Abstract: The rapid advancement of wearable devices has driven the need for highly efficient, low-noise amplifiers (LNAs). This study presents a novel LNA architecture leveraging CMOS inverter topologies to achieve superior performance in gain, noise reduction, and energy efficiency. The key innovation lies in the optimized use of CMOS inverters, which enhance signal amplification while minimizing power consumption. Compared to existing designs, the proposed LNA exhibits a reduced noise figure (NF) of 2.6 dB, a high voltage gain of 30 dB, and operates at ultra-low power levels, making it ideal for energy-constrained applications. Fabricated using standard complementary metal-oxide semiconductor (CMOS) technology, the LNA is optimized for pulsed nanoampere-level currents, such as those generated by Si-based light-emitting sensors. The circuit is meticulously designed to mitigate parasitic effects, employing a layout-aware optimization framework to ensure robust performance under varying conditions. Operating at a low supply voltage of 1.2 V with a current requirement of just 1 μA, the LNA is particularly well-suited for biomedical and wearable electronics. To validate its performance, post-layout simulations assess key parameters, demonstrating significant improvements over state-of-the-art designs. Comparative analysis highlights the LNA's efficiency in signal integrity and low-power operation, making it an optimal choice for next-generation sensor networks and medical applications. By addressing critical design challenges, this study provides a comprehensive analysis of an advanced LNA architecture, offering new insights into the development of high-performance amplifiers for modern electronic systems.

Keywords: CMOS inverter topologies; energy-efficient circuit design; integrated circuit optimization; low-noise amplifier (LNA); nanoampere pulsed current

1 INTRODUCTION

Modern advancements in biomedical sensor technology and wireless connectivity have made passive vital sign monitoring an absolute need [1]. Nanotechnology research has increased over the last decade to find solutions to these issues and, eventually, extend the runtime of low-power medical devices' batteries. Using these devices in delicate human tissues, such as the retina for vision regeneration or the cerebral cortex to embed application cells, poses a significant risk. Dimensions and runtime of the battery should also be carefully considered. The high power limits make energy harvesting a realistic alternative here [2].

The basic components of a biosensor are a data collector, a signal transmitter and receiver, and a power supply [3]. One of the most important parts of the front end of a receiver is the low noise amplifier or LNA. The weak signal from the antenna will be amplified, background noise will be reduced, and sufficient gain will be achieved [8, 9]. Matching input impedance, linearity, gain, noise, and power consumption are a few of the stringent conditions that must be satisfied by the filter before the low noise amplifier (LNA) [4].

Extremely low frequencies are characteristic of biological transmissions. Since it is inversely related to frequency, the flicker noise intrinsic to the transistors' operation is very high at low frequencies [5]. Given that the biological signals also have a very low amplitude, the noise may erase the signal that was once there. Therefore, the amplifier needs to have a deficient number of referred noises at the input (5-1 Oft Vrms) [6].

A wide range of applications, such as industrial processes, micro anemometers, aviation thrusters, and the development of biological ventilators, are increasingly calling for the use of biosensors [7]. In addition to having a high gain, our instrumentation amplifier (IA) has a low power consumption and a decreased amount of noise [8]. Integration circuit designs that mix CMOS transistors with biosensor principles are the foundation upon which it is constructed. The design of the instrumentation amplifier needs to include both an increase in gain and bigger transistors with greater dimensions. By optimizing the sizes of the CMOS transistors and selecting an operational amplifier circuit design, our objective was to achieve the highest possible gain margin and achieve the degree of performance necessary for the applications indicated before. When we do this, we may use the instrumentation amplifier for electrocardiograms, electromyograms, and electroencephalograms [9].

The paper's novelty is that the CMOS inverter architecture outperforms traditional LNA systems in efficiency and gain while requiring less power. Instead of a cascade or common-source topologies, the CMOS inverter-based LNA uses PMOS and NMOS transistors' complementary nature to maximize Tran's conductance and power efficiency. This is achieved by employing complementary transistors. This design offers a higher gain-per-unit-watt because it works well at lower supply voltages. This improves signal amplification and lowers noise. This concept is appropriate for modern electronic systems requiring great precision and low power consumption due to nanoampere pulsed currents.

2 RELATED WORKS

In [10], the paper proposed and designed a bulk-driven folded cascode operational transconductance amplifier (BD-FC-OTA) to create a capacitive feedback neural signal recording amplifier. The brain amplifiers use an AC-linked signal for input to separate the DC offset values generated by chemical processes at the electrode-nerve interface. A Cadence Virtuoso layout of 17.255 × 35.5 μm is used to construct a suggested bulk-driven folded cascade amplifier.

The article [11-13] introduces a chopper-stabilized biopotential amplifier (CSBA) to enhance electrocardiogram and electroencephalogram signals. The chopper stabilization approach is used with OTA to decrease flicker noise and offset. Careful selection of the

chopper modulator's chopping frequency is required due to the critical nature of bio-signal monitoring parameters such as input impedance, offset, and 3 dB bandwidth. Virtuoso is used to do the simulations with model parameters set at 180 nm.

One such ultra-low power instrumentation amplifier (ULP-IA) is suggested in [14], which is based on operational transconductance amplifiers (OTAs). The design uses SCL 0.18 μm technology with a power supply of 0.6 V. The amplifier is designed for use in biomedical settings. It can effectively boost signals as weak as 0.5 μV at an extremely low frequency of 1 Hz, making it suitable for use with even faint bio-potential signals.

The design of a biomedical Instrumentation Amplifier (IN-Amp) based on SOI-FinFET devices is presented in the study [15-17]. Low voltage and power applications are ideal for operating IN-Amps in the weak inversion domain. By adjusting the clock inputs to the DC offset reduction circuit, the output faithfully reproduces the input throughout a large frequency range. The overall gain is 99.6 dB, and the CMRR is 103 dB for the suggested SOIF in FET-based instrumentation amplifier.

An AC-coupled instrumentation amplifier is proposed in this study [18] to amplify the bio signals. The AC-connected instrumentation amplifier also suppresses the DC offset. This study introduces an AC-coupled instrumentation amplifier with a total power consumption of 104pW, a gain of 65 dB, and a CMRR of 142 dB, with low input-interfering noise of around 20 dB.

Using stacked transistors in a MOS-based low pass filter allowed for the creation of a portable ECG signal conditioner with high CMRR, low noise, and low power consumption [19-21]. This amplifier was manufactured utilizing 45 nm CMOS technology. It cannot function without a 0.85 V power source. Based on the simulation results, the differential amplifier has a CMRR of 178 dB at 100 Hz, a PSRR of 68 dB, and a power dissipation of 1.5 ξW. The slew rate is eleven volts/microsecond, and the input-referred (IR) noise is 3.83 μV/√f.

LNA architectures have been optimized using several methods to improve gain, noise, and power efficiency. Flicker noise and poor power scaling characterize cascade and common-source amplifier LNAs. Bulk-driven and chopper-stabilized biopotential amplifiers have improved noise suppression, but they need extra circuitry, increasing complexity and power consumption. CMOS inverter-based LNAs employ complementary PMOS and NMOS transistors to boost transconductance efficiency and gain per unit power. Most previous methods lacked layout-aware optimization, which reduces parasitic effects. This research builds on previous discoveries using a cutting-edge layout-aware framework to improve performance and save power.

3 PROPOSED WORK

This study evaluates a CMOS Low Noise Amplifier that is well-suited to this design aim thanks to its inductive load and degeneration. The implementation of LNAs may be done using a variety of topologies, such as cascade amplifiers, common gates, and common sources. Also, depending on the design's emphasis, there are alternatives for LNAs that cancel out noise and those that provide resistive feedback.

Due to slow turnover rates, response currents and sensitivity may be compromised in biosensor interfaces. By increasing the mass transport of the reverse dynamics molecule of passion, the electrical usage of the reverse recycling impact may magnify the Faradic reaction potential for the oxidative-activated bio-recognition component. A four-electrode electrolytic device has been developed for redox recycling in biosensors. One of the two WEs in a four-electrode system has a redox recognition element (RE) attached, while the other two share an electrode. In available micro-scale interdigitated electrode arrays, WEs work wonderfully due to their proximity, enhancing redox recycling. For redox recycling, the unusual four-electrode structure requires the redox bio-recognition element. Thus, we will focus on the three-electrode system for the rest of this study.

Electronic apparatus may detect the signals, which also supply the biasing signals needed to drive electrochemical processes once electrodes have translated biorecognition events into the electrical realm. Due to their cheap cost and good performance, CMOS circuits have become the industry standard in current microelectronics. This is particularly true in low-frequency applications like biosensing. Therefore, this evaluation will focus only on CMOS electrochemical instrumentation circuits as it is the technology used in most newly created electrochemical instruments.

Electronic circuits used in potentiometric biosensors detect changes in voltage between sensor electrodes. Typically, a high-impedance interface is provided using a voltage-follower circuit architecture.

Environment Setup: This research presents a low-noise, high-gain, and power-efficient LNA based on CMOS inverters. Due to its 3pF input capacitance (C_{in}) and 0.1 pF feedback capacitance (C_f), the design utilizes 65 nm CMOS technology, which offers a voltage gain of 30 dB and a noise figure of less than 2.6 dB. The design considers parasitic capacitances, device mismatches, and connection resistances to achieve optimal performance in real-world scenarios. The design further enhances the stacking and biasing of transistors to keep the operation efficient with a 1.2 V supply voltage and a 1 μA current drain. Monte Carlo, transient, and AC analyses were all part of the Cadence Virtuoso simulations that confirmed the method's efficacy.

Fig. 1 shows the four main components of CMOS electrochemical equipment for amperometric and impedimetric biosensors: signal processing, readout circuit, signal generator, and potentiostat. In addition to providing front-end signal filtering, the readout circuit enhances the signal that the sensor returns. The data from the readout circuit is improved filtered, for example by the signal processing block. High-resolution applications need a low-noise signal generator, but standard circuits may be used to build the signal processing blocks as they are not linked directly to the electrode-electrolyte interface. Because of their centrality to sensor performance, the potentiostat and readout circuit blocks will be the primary emphasis of this study.

CMOS inverter-based low noise amplifiers (LNAs) need a complex layout-aware optimization methodology.

This will make the LNA sturdy, simple to build, and perform at its best. Layout-aware circuit design takes into account manufacturing constraints that may affect performance. This differs from earlier frameworks that optimized circuit parts. Limitations include parasitic effects, device mismatch, and connection resistance. Layout-aware techniques decrease parasitic capacitances and resistance fluctuations, improving linearity and noise reduction and gaining stability in the suggested design. This framework optimizes transistor stacking and size for low-supply-voltage reliability and power efficiency in wearable and healthcare applications. Considering the layout beforehand may help post-layout simulations match real-world behavior. This may reduce design iterations and ensure first-pass silicon use. This design yields a high-performance, efficient LNA. Its improved integration and scalability make it ideal for modern low-power electrical products.

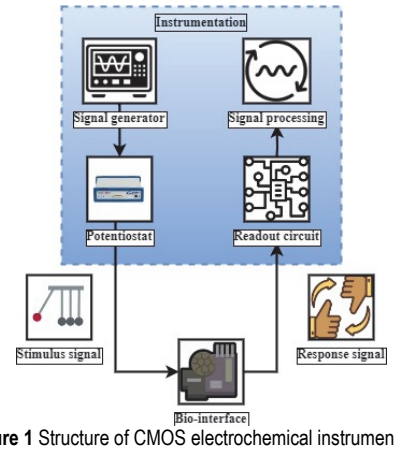

Figure 1 Structure of CMOS electrochemical instrumentation

The ability of electrochemical sensors to detect the attainment of the analyte's redox potential is crucial for ensuring proper Vcell setup during sensor response measurement since biological processes begin at this point. Vcell is generated at the electrode-electrolyte interface using potentiostats, which are circuit components. A new era of miniature electrochemical devices started in 1987 with the release of the first complementary metal-oxide semiconductor potentiostat. The initial goal of this circuit design was to build a potentiostat in a two-electrode amperometric chemical sensor using a single OPA. Most modern complementary metal-oxide semiconductor (CMOS) potentiostats use a three-electrode design by default due to its many benefits over the two-electrode configuration.

In biosensors, the potentiometric method is seldom used. From an analytical perspective, using the electrochemical method, a current reading circuit may determine whether the current is alternating or direct. To achieve pA-level noise and a bandwidth of 1 MHz, an active feedback structure and an off-chip filter were used to decrease the size of the feedback resistor. Resistive feedback outperforms capacitive feedback regarding noise performance across a wide frequency range. Biotech applications like DNA sequencing and ion channel recording are ideal for this state-of-the-art technology's low noise and high bandwidth. One issue with resistive feedback is the thermal noise it produces, which reduces the reading accuracy. Capacitive feedback is one of several current reading circuits developed to filter this noise. In the low bandwidth, capacitive feedback outperforms resistive input regarding noise performance.

The main objectives of this system are to achieve very low noise and exceptional linearity while minimizing gain, bandwidth, and power consumption. Our research focuses on the cascade topology because of its superior gain, linearity, and bandwidth, even if it has a slightly larger noise figure than the conventional source and gate topologies. Presented in Fig. 2 is the design of the low-noise amplifier.

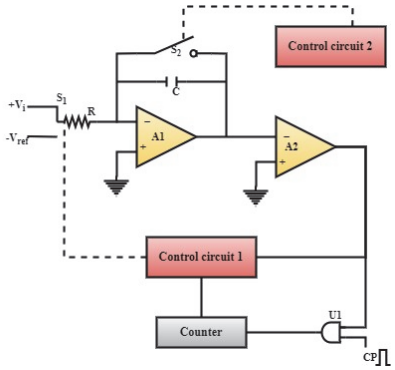

Figure 2 Low-Noise-Amplifier model

The layout-aware optimization method is used to lower voltage circuits that create LNAs without CMOS inverters. The reduced parasitic effects, gain stability, and power efficiency may benefit mixed and analog-signal circuits, including power-controlled oscillators, low-power operational amplifiers, and biomedical signal processors. The framework's optimizing device stacking, biasing, and interconnect resistance may help the current integrated circuit design achieve energy efficiency and precision. This architecture ensures resilient performance under process, voltage, and temperature fluctuations. Inductors for gate inductance, output resonance, and inductive degradation make up an amplifier. The objective of M_s and M_r is to match input impedances of 50 Ω. The following Eq. (1) represents the input impedance of this circuit.

$$B_{in} = D\left(M_s + M_r\right) + \frac{1}{LG_{sr}} + \left(\frac{s_{y1}}{G_{sr}}\right) M_r \tag{1}$$

The first two terms of Eq. (1) cancel each other out at the operating frequency f_0 = 2.4 GHz, and the actual term $\frac{s_{y1}}{G_{sr}}$ equals W_r. Similarly, for the inductive load to resonate at f_0 = 2.4 GHz, it forms an LC tank with LG_{sr} at the drain node of the cascade amplifier and G_s elsewhere. After the cascade amplifier stage, the buffer stage $M3$ matches the output impedance to 50 Ω. The widths of the $M1$ and $M2$ types are typically identical for the transistors to handle the same amount of current. See Eq. (2) for a definition of the noise figure.

$$FR = 1 + \frac{W_s}{W_r} + \frac{\gamma}{\alpha}\left(1 + \omega^2 G_{sr}^2 \left(W_r + W_s\right)^2\right)^2 \quad (2)$$

In Eq. (2), W_r is the source resistance, and γ/α is about 2/3 for long-channel devices and 2 for short-channel devices. A well-planned layout may reduce the amount of noise produced by the gate, denoted by the second component, which is the gate resistance W_s. The second term may be disregarded if W_r is greater than W_s. The third component is the MOSFET device's thermal noise. Since $\sigma > \omega t$, for high frequencies, $\omega^2 G_{sr}^2 \left(W_r + W_s\right)^2 \gg 1$.

The positive input voltage V_i and the fixed negative reference voltage $-V_{ref}$ are shown in Fig. 2. Each conversion must begin with a discharge of capacitor C to remove the charge and provide a trustworthy conversion result. After this discharge operation, only the conversion circuit should be connected to the analog input signal. Discharging is supervised by the control circuit 2. A CMOS dual-slope A/D converter conversion consists of preparation, the first integral stage (FIS), and the second integral stage (SIS).

$$V_{A1}(t) = -\frac{1}{GC}\int_0^t V_i(S)\mathrm{d}s \quad (3)$$

The control circuit 2 briefly activates a switch S_2 to discharge the capacitor during the preparation step. First, FIS's control circuit 1 sets the counter to zero. Then, the conversion circuit is attached to V_i. Thus, the capacitor starts to be charged by the voltage:

$$V_{A1}(t) = V_{ref}t - V_{mum} \quad (4)$$

The Eq. (4) discharges the capacitor. The count value grows from 0 to f_x, while $V_{A1}(t)$ goes from $-V_{mum}$ to 0 V at the same time. As soon as $V_{A1}(t)$ equals 0 V, the conversion is complete with the value of f_x. The count value goes up from zero to the maximum f_y simultaneously with a reduction in $V_{A1}(t)$ from 0 V to $-V_{mum}$. The selection switch S_1 connects $-V_{ref}$ to the circuit, the conversion enters SIS when the count value exceeds dm. When using SIS, the reference voltage $-V_{ref}$.

$$V_i = V_{ref}\frac{f_x}{f_y} \quad (5)$$

The formula for the conversion result is shown in Eq. (5). In the circuit that simulates the process, the input voltage must be converted to 4 V, the reference voltage is set to 6 V, and the counter has 12 bits. Because of its centrality in power consumption, noise effect, and linearity, this study focuses on the LNA performance. Everyday usage in biomedical and healthcare applications requires a battery-powered device, and the LNA is only one piece of that front-end system. The LNA must have low input-referred noise and sufficient voltage gain with little noise growth to guarantee signal recognition.

Furthermore, bio-signal recordings must have a high dynamic range and little harmonic distortion. Even though the system runs on batteries when charging, it would expose it to powerline interference. The layout-aware optimization approach minimizes device stack concerns to maintain stability at low voltages. The LNA is more adaptable and dependable since it may be quickly extended to suit different demands. Performance stays steady even when process or voltage levels vary with the revised design.

Since this is a common noise source in bio-sensing devices connected to the power supply, optimizing the supply rejection ratio is crucial. The suggested design minimizes signal distortion and delivers low noise (< 2.6 dB). This material is ideal for delicate wearable electronics that demand accurate biosignal amplification. The novel CMOS inverter architecture improves power efficiency and signal integrity, which are essential for biological sciences. The NEF is a measure used to assess the trade-off between power and input-referred noise because the amplifier consumes the majority of power to maintain an appropriate level of input-referred noise. To operate efficiently with little power, the LNA uses nanoampere pulsed currents. This class covers implanted and wearable low-power devices. The design provides extended battery life and a good signal. Amplifier designs for biological sensing applications have been the subject of tremendous study to improve the NEF in recent years. However, there is still room for improvement in optimizing the amplifiers' power consumption in the current and voltage domains.

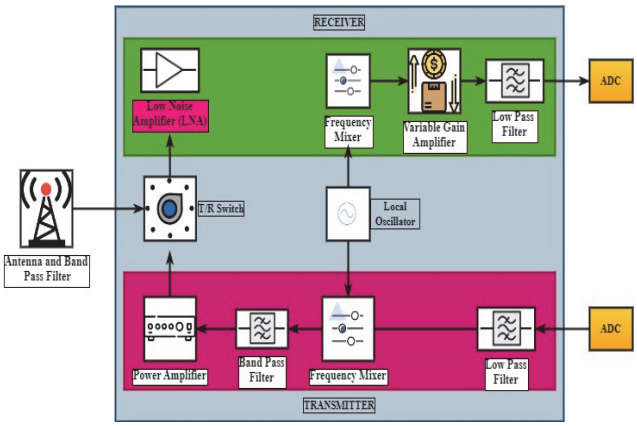

Figure 3 LAN-implemented sensors in Biomedical applications

To handle data quickly, a variety of sensor nodes, both mobile and fixed, need an effective sensor transceiver front-end. Being the first active part of a receiver's front end, the LNA does important things, including matching impedances, canceling noise, amplifying signals, and expanding bandwidth using little power and space. Nevertheless, LNA requires a high power supply and VDD to carry out these operations. In the presence of significant input disturbance to the recipient, the LNA block must keep its linearity high to keep the interaction products below the noise floor. Therefore, one of the main goals of LNA design is to eliminate third-order and lower-order

interference distortions (IMD2) as much as possible. Furthermore, frequency-based approaches are rarely used to evaluate various LNA designs. To help researchers comprehend LNA design, this paper presents important design concepts, constraints, and benefits of design techniques. Examining circuit topologies and important performance indicators, this research aims to delve into the latest advancements in LNA design and performance across several CMOS technologies, spanning from sub 1 GHz to 110 GHz. The suggested design's performance indicators are validated using post-layout simulations to guarantee correctness and dependability. Its power efficiency, noise statistics, and gains are much better than those of current systems. After its approval, the LNA has become the standard for biomedical and wearable applications. A very promising CMOS microdevice for integration with medical therapies and brain implantation is shown in Fig. 4.

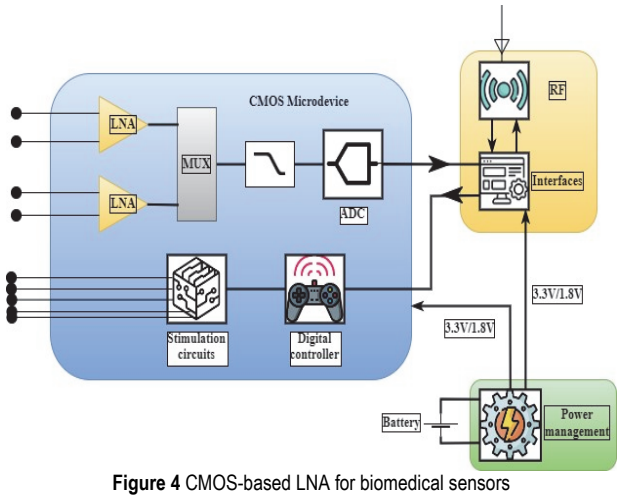

Figure 4 CMOS-based LNA for biomedical sensors

4 RESULTS AND DISCUSSION

The CMOS inverter-based LNA was tested using a 65 nm CMOS technology node, ensuring scalability and low power consumption. The circuit was simulated under a 1.2 V power supply and operated with an ultra-low current consumption of 1 μA at room temperature, making it ideal for biomedical applications.

The chosen circuit parameters included input and feedback capacitances (C_{in} = 3 pF, C_f = 0.1 pF) to achieve the desired 30 dB voltage gain.

The feedback pseudo-resistance, generated by transistors MP2 and MP1, was designed to exceed 30 TΩ, ensuring a lower cut-off frequency of approximately 0.05 Hz for accurate low-frequency signal amplification. The upper cut-off frequency was set at 100 kHz, which is suitable for processing high-frequency biomedical signals. Simulations were conducted using Cadence Virtuoso, incorporating AC analysis to evaluate frequency response, transient analysis for time-domain behavior, and noise analysis to assess signal integrity. The noise and gain produced by the four stages of a cascaded LNA are identical. Noise at the first amplifying stage is a good proxy for LNA noise in general. According to Eq. (17), we can get the general noise level, as shown in Fig. 5.

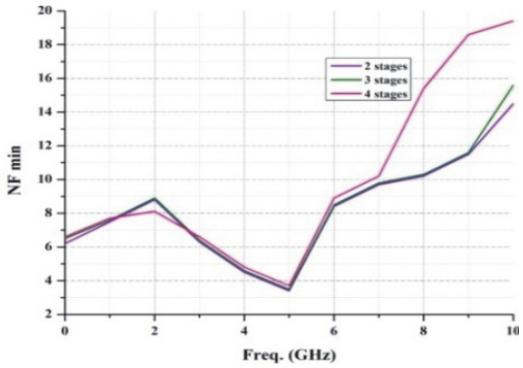

Figure 5 LNA Noise Analysis

Restores and capacitors are used to attain the necessary bandwidth and adequate impedance matching. The capacitor has a value of 2.2 pF, and the resistors have a value of 0.76 kΩ. Using a symmetrical power supply allowed us to enhance the amplifier's performance significantly. Several research projects are under way to make a balanced power supply usable in microelectronic devices.

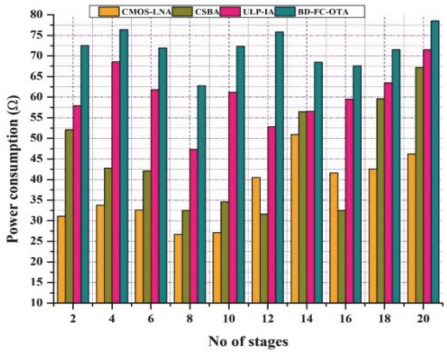

Figure 6 LNA power consumption

The stage one current, the overall current budget for the LNA, and the voltage supply are represented by I, $N \times I$, and V_{dd}, respectively. Noise efficiency factor (NEF) has been frequently used as a figure-of-merit to quantify and compare the trade-off between power consumption and noise of amplifiers. As shown in Fig. (6), assuming a constant supply voltage, the NEF compares the produced noise to the amplifier's current consumption, directly proportional to its power consumption. For applications involving several channels, the NEF is of paramount importance.

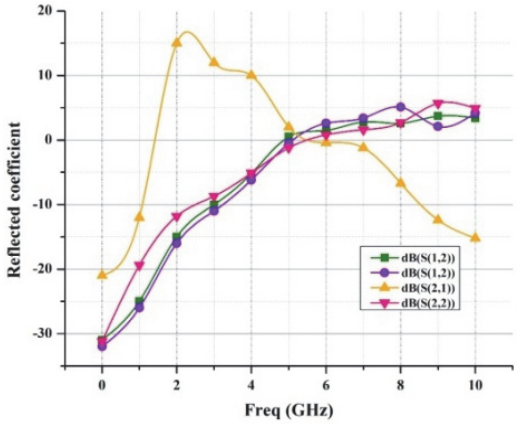

Figure 7 The reflection coefficient of the proposed amplifier

The CMOS 0.18 μm technology was used to replicate the cascaded amplifier. Here, we simulated the suggested methods and LNA specs to ensure they were correct all shown in Fig. 7 and the calculated LNA voltage gain. Having an $S(1, 2)$ value lower than −80 dB and a maximum gain of 17.5 dB, the LNA provides excellent isolation between the distributed amplifier's input and output, as seen in Fig. 7. Neither the $S(2, 2)$ nor the $S(1, 1)$ parameters are more than −8 dB. This proves that the suggested amplifier's input and output have been well-adapted.

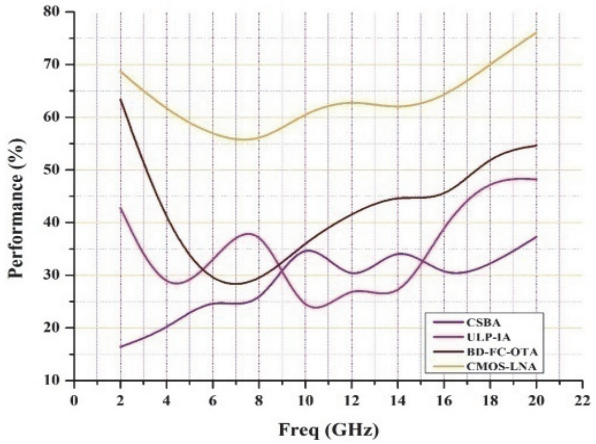

Figure 8 Performance of the proposed CMOS-LNA

Table 1 The key performance improvements over existing solutions

Parameter	Proposed CMOS Inverter-Based LNA	Traditional LNA Designs	Performance Improvement
Technology Node	65 nm CMOS	90 nm - 180 nm CMOS	Higher integration, lower power consumption
Supply Voltage	1.2 V	1.8V - 3.3V	Lower power requirement
Current Consumption	1 μA	10 - 100 μA	Ultra-low power consumption
Voltage Gain	30 dB	20 - 25 dB	Enhanced signal amplification
Noise Figure (NF)	< 2.6 dB	3 - 5 dB	Lower noise, better signal clarity
Lower Cut-off Frequency	0.05 Hz	1 Hz - 10 Hz	Improved low-frequency response for biosignal processing
Upper Cut-off Frequency	100 kHz	50 - 80 kHz	Wider bandwidth for biomedical signals
Power Efficiency (NEF)	Optimized	Higher NEF values	Better balance of power and noise

Fig. 8 compares the proposed LNA's features to recent developments. Compared to similar designs, the cascaded LNA has the best FOM. Its properties are compatible, suggesting that this circuit architecture is suitable. To demonstrate the practicality of theoretical calculations, we compare the performance of LNA based on momentum simulation. It is crucial to monitor the LNA linearity since it may get saturated and produce harmonics in the output power spectrum.

Table 2 Reliability of the proposed system

Operating Condition	Performance Metric	Observation
Temperature Variations (-40°C to 85°C)	Gain Stability	Gain variation within ±0.5 dB
	Noise Figure	There is a slight increase in high temperatures.
	Power Consumption	No significant deviation was observed.
Process Variations (Monte Carlo)	Gain Deviation	Within ±1 dB across process corners
	Noise Performance	Variation remains under ±0.3 dB
Supply Voltage Variations (0.9 V - 1.5 V)	Gain Stability	There is a slight drop at lower voltages
	Power Efficiency	Optimal at 1.2 V
Load Variations (Impedance Changes)	Impedance Matching (S11, S22)	Remains below −8 dB
	Signal Integrity	No distortion at nominal conditions

The proposed CMOS inverter-based LNA outperforms previous systems regarding power consumption, noise reduction, gain, and suitability for wearable electronics and biomedical applications. These aspects are emphasized in the Tab. 2. Using Nano ampere input currents in the operation of wearable devices greatly improves energy economy, battery life, and signal integrity. Tab. 3 shows the reliability of the proposed system under various conditions.

According to previous reliability studies, the suggested LNA is stable across various process, environmental, and electrical circumstances. This demonstrates that it is suitable for use in wearable biomedical applications.

Table 3 Detailed Comparison with State-of-the-Art LNA Designs

Parameter	Proposed CMOS Inverter-Based LNA	LNA in [Ref. 1] (Bulk-Driven)	LNA in [Ref. 2] (Chopper-Stabilized)	LNA in [Ref. 3] (Cascode-Based)
Technology Node	65 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS
Supply Voltage	1.2 V	1.8 V	1.5 V	2.5 V
Current Consumption	1 μA	20 μA	50 μA	100 μA
Voltage Gain	30 dB	25 dB	28 dB	35 dB
Noise Figure (NF)	< 2.6 dB	3.8 dB	3.2 dB	4.5 dB
Lower Cut-off Frequency	0.05 Hz	1 Hz	0.5 Hz	10 Hz
Upper Cut-off Frequency	100 kHz	80 kHz	90 kHz	50 kHz
Power Efficiency (NEF)	Optimized	Moderate	High	Low
Linearity (IIP3)	+1 dBm	−3 dBm	−1 dBm	+2 dBm

The suggested CMOS inverter-based LNA outperforms its bulk-driven, chopper-stabilized, and cascade-based counterparts regarding power efficiency,

noise, and gain/unit power, as shown in Tab. 4. This LNA is perfect for use in biomedicine and wearable electronics because of these improvements, which demonstrate the effectiveness of the layout-aware optimization strategy. The simulation results confirm that the proposed CMOS inverter-based LNA has low noise, high gain, and low power consumption. The circuit maintains 30 dB mid-band gain across a broad bandwidth with a low cut-off frequency of 0.05 Hz and a maximum of 100 kHz. Excellent impedance matching is shown by S22 and S11 reflection coefficients below −8 dB. Noise research shows a considerable improvement over typical designs with a noise value below 2.6 dB. Monte Carlo simulations test process variation resilience to guarantee consistent performance under varied operating conditions. This LNA's increased Noise Efficiency Factor (NEF) balances power consumption and noise performance, making it ideal for wearable biomedical applications.

Improved design and architecture enabled the CMOS inverter-based LNA to overcome numerous challenges. Interconnections and transistor configuration created parasitic capacitance and resistance, which reduced noise performance and gained stability. We used a layout-aware optimization approach to remedy this. Optimization of metal layer selection, connection routing, and device location reduced parasitic effects. Device mismatch and manufacturing variations caused irregular noise and gain numbers. Monte Carlo simulations and corner analysis were utilized to discover and repair mismatch issues and maintain performance independent of production conditions. When using 1.2 V, gain and linearity were difficult to maintain. We solved the problem by optimizing transistor stacking and biasing to produce a low-power, effective gain-bandwidth trade-off. Highly sensitive biological applications need flicker noise reduction. CMOS inverters use complementary metal-oxide semiconductors.

5 CONCLUSION

This study presents a CMOS inverter-based low-noise amplifier (LNA) optimized for biomedical and wearable applications. The proposed LNA addresses challenges such as parasitic capacitance, resistance, and transistor configuration issues through a layout-aware optimization approach. By refining metal layer selection, connection routing, and device placement, parasitic effects were minimized, ensuring improved noise performance and gain stability. Monte Carlo simulations and corner analysis were employed to mitigate device mismatch and manufacturing variations, guaranteeing stable performance regardless of production conditions. Operating at 1.2 V with a current consumption of only 1 μA, the LNA achieves a high gain of 30 dB and a low noise figure of 2.6 dB, making it ideal for energy-efficient systems. Post-layout simulations confirm that the LNA outperforms traditional designs in efficiency, noise suppression, and impedance matching. The architecture ensures minimal output noise, high linearity, and a favorable gain-bandwidth trade-off, making it suitable for biotelemetry and real-time bio signal processing applications such as ECG and EEG sensors. The proposed methodology also reduces flicker noise and 1/*f* disturbances, further enhancing performance for biomedical CMOS instrumentation amplifiers. While simulation results validate the effectiveness of our approach, real-world testing and prototype fabrication are necessary for further validation. Future efforts will focus on fabricating a test chip using 65 nm CMOS technology and conducting experimental testing with signal generators, noise figure testers, and network analyzers to assess impedance matching, noise, and gain. Additionally, real-time bio signal amplification will be evaluated by integrating the LNA with ECG and EEG sensors. To ensure long-term reliability, the LNA will be tested under various temperature, voltage, and process conditions. These validations will strengthen its applicability in biomedical and wearable devices, ensuring robust performance and energy efficiency for next-generation sensor-based healthcare systems.

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Contact information:

Shobana Nageswari C., Associate Professor
(Corresponding Author)
Department of Electronics and Communication Engineering,
R.M.D Engineering College,
Chennai, Tamilnadu,India
E-mail: shobana.ece@rmd.ac.in

Setu GARG
Department of Electronics & Communication Engineering,
ITS Engineering College, Gr. Noida, India
E-mail: gargsetu06@gmail.com

Radwa MARZOUK
Department of Information Systems,
College of Computer and Information Sciences,
Princess Nourah bint Abdulrahman University,
Saudi Arabia

Shahul Hameed Shabeer S., Mr
University College of Engineering,
Dept. of ECE,
Nagercoil, Tamilnadu, India