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Original scientific paper

Performance Enhanced Penta-MTJ Based Logic Gates Using FinFET for Low Power and High-Speed Applications

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Abstract: The performance of conventional CMOS circuits can be enhanced using advanced devices and technologies to address the growing gap between device fabrication and computing system design. Spintronic devices, particularly magnetic tunnel junctions (MTJs), have emerged as a promising solution for improving CMOS performance by offering faster execution, lower power consumption, and infinite endurance. MTJs are highly suitable for designing and implementing memory and logic circuits. This paper introduces the implementation of a PentaMTJ-based logic gate using FinFET technology. The proposed design features self-referencing, cascading capability, and operation at reduced voltage levels, effectively eliminating the headroom issue in pre-charge sense amplifiers. The proposed architecture ensures faster reading and writing operations while minimizing power consumption and leakage currents due to the FinFET-based design. To validate the functionality of the MTJ device, a BRAUN multiplier is cascaded with a shift register using MTJ technology. Comparative analysis indicates that MTJ devices offer superior cascading performance, reduced static power dissipation, and lower voltage headroom. The implementation and simulation were conducted using the Synopsys Analog Design Module.

Keywords: FinFET Technology; CMOS performance enhancement; low power design; magnetic tunnel junction (MTJ); penta-MTJ

1 INTRODUCTION

Power consumption in integrated circuits is to be optimized in electronics design. While considering VLSI design it plays a key role. In VLSI circuit, power consumption is caused by various parameters like short circuit, second order effect and so on. Once this problem is rectified the designed circuit becomes the efficient one. For application where memory requirements are higher like the digital signal processing, spintronic devices are advantages. The literature has shown that the Magnetic tunnel junctions (MTJ) are used in random access memories. These MTJs find applications which have nonvolatile logic fan-outs. The junction devices are faster in reading and writing data with minimum power requirements. Combining MTJs with multigate devices will open new doors in design. In the advent of System On Chip architectures where miniaturization of devices with large magnetic memory is required, MTJs play an important place. The fabrication needs ferromagnetic layers with different coercivities. The insulating barrier is sandwiched between the ferromagnetic layers of different coercivities [1-3].

Fig. 1 shows the various layers of the typical MTJ. The layers are shown clearly to visualize the electron flow in the barrier. Several barrier materials are chosen, for example ZnO, Al2O3, NaCl and MgO. Even ferrites and titanates were used as barrier layer material. The insulating layer is of graphene type material. The Fe. CoFeB are used for ferromagnetic layers. The speed of operation affects the power consumption and delay. As in conventional CMOS circuits the speed also affects the power and delay. Sometimes the CMOS finds low power at very high frequency compared to MTJ devices. The structure of the PentaMTJ and magnetic tunnel junction is shown in Fig. 1. The spin dependent tunneling through insulating barrier is the phenomenon of the fabrication. Micrometer scaling makes the device small and advantage to be used in memories. The device will work for a long period of time. The data retention is higher through thermal stability. For the barrier parameters, a definite value for the resistance of junction area is maintained if MTJ is to be used in memories. In addition the junction characteristics of the MTJ are studied from the junction area and barrier resistance. In digital logic design using CMOS, electrical charge determines the logics in terms of voltage VDD or ground. The spin of electron in up and down movement determines the logic in Spintronics. It works on the principle of tunnel magneto resistance (TMR). The oxide layer separates the layers made of ferromagnetic material. The power consumption and delay can be improved using the oxide layer in between the layers. The other way of fabrication is the 3-D backend integration process. The PentaMTJ-based logic gate is different from other devices due to its cascading features [4-7]. The circuit implemented will prove better swing and supply voltage headroom. In recent times

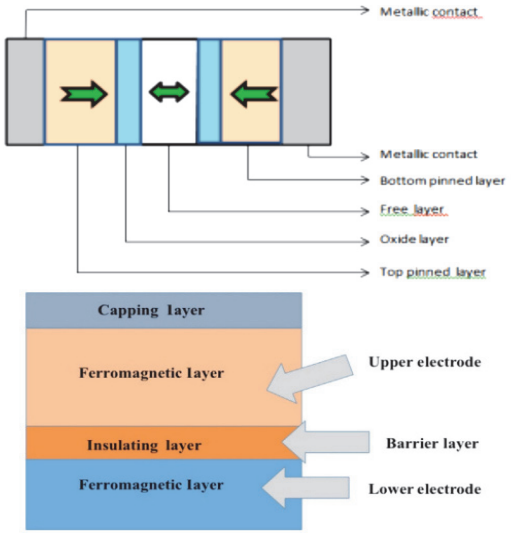

Figure 1 Structure of PentaMTJ and Schematic of magnetic tunnel junction

MTJs were used for magnetic random-access memory (MRAM) design. Combination and sequentiial circuits can be implemented using MTJ. The previous research used CMOS and MTJ structures combined in 130 nm technology. The higher technology was chosen to maintain speed and wide frequency response. But power consumption increases as the frequency increases. But in

lower technologies below 90 nm the power is drastically reduced but with the limitation of frequencies [8-10].

The sequential circuits like flip-flop, register, latches etc play important role in microprocessor and memory designs. The CMOS-MTJ counterparts in magnetic arithmetic logic unit (MALU) with logic-in-memory (LIM) structure consume less standby power dissipation. But for higher frequencies the devices suffer from leakage current. Compared to CMOS the MTJ-CMOS is better in performance but spintronics devices using FinFET will perform better. The scaling technology in CMOS led to ultra low power with near threshold operation. But leakage is problem for second order effects. Spintronic devices if implemented in FinFET will perform better. This has motivated to enhance and do work which is presented in this work. The motivation of the work is to utilize electron charge and the electron intrinsic spin of MTJ to develop sequential and other digital circuits. It is found to be the most suitable compared to the rest of the spintronic devices.

2 LITERATURE REVIEW

In literature several works were carried out for the investigation of magnetic tunnel junction (MTJ)-based circuits. Those works focus on the development of communication between devices, circuits, logic circuits and devices. Few studies were carried out based on analysis, and are presented below. For instance the design focused on the performance analysis of magneto resistive RAM, content addressable memory (CAM) and ternary CAM (TCAM). The work was focused on the MTJs current sensing properties in memory devices. The work extends the performance evaluation for volatile and nonvolatile systems. The CMOS based BJT was implemented in the 180nm with 5V supply. The power consumption was high when compared to the technology addressed today. The differential 2-Transistor 2-MTJ (2T2MTJ) cell with the conventional device. The three-terminal Magnetic Tunnel Junction (MTJ) for memory has improved immunity towards the read errors. In-Plane Anisotropy (IPA) for MTJ and differential 2-Transistor 2-MTJ cell was performed. These studies may be applied for MTJ design for Random Access Memory [11-13].

The circuits like Multi-bit magnetic adder (MA) were designed using MTJ. and the data was stored in perpendicular magnetic anisotropy (PMA) memory. In recent times several logic circuits were developed which can be hydridized using MTJs [6-10]. The challenges in the CMOS integrated circuit (VLSI) design due to reliability issues are rectified using Magnetic tunnel junction (MTJ). The write operation and data sensing consume optimum power. The two-in-one (TIO) MTJ cell and Radiation-induced single event upset were addressed. Combinatory circuits were implemented but they consume more power than the magnetic tunnel junction (MTJ). The demonstration presented the magnetoresistive layers' interaction on an inhomogeneous magnetic field of MTJ. For output sensitivity improvement the NDT bridge circuit is designed using MTJ. The full-bridge circuit is designed using MTJ sensors, and resistors. A sensitivity of 0.135 mV/mT is achieved [14-16].

An amorphous electrode using magnetic tunnel junctions (MTJs) was designed. In addition the authors designed a MgO barrier layer and through annealing process in the electrode device a linear resistance was obtained. The design reported a tunnel magnetoresistance ratio with optimistic anisotropy field response. For low frequencies biomedical applications, the Ultrasensitive magnetic field sensors were used. The linearity is improved using large area magnetic tunnel junction (MTJ) sensors combined with permanent magnets. Soft ferromagnetic flux guides (FG) were used for sensitivity improvements. The investigation compared MgO-based MTJ with various flux guides.

A similar principle of tunnel magneto-resistance based sensors was utilized for the Magnetocardiography (MCG) analysis. The heart functions especially the R and QRS complex were detected using the low noise amplifiers. Averaging was exempted for R detection while the same was adopted for QRS complex detection. The work focused on the improvement of sensitivity of MTJ using double gap device. The investigation shows that magnetic magnification in double-gap MFC increases and sensitivity can be doubled. The noise occuring in conventional circuit is difficult to remove compared to MTJ device [17, 18].

In magnetoresistive sensors using MTJs, the small variation in magnetic field can be detected. The aspect ratio of the sensors and junction areas can be varied according to the aplication. MTJ geometry affects the sensitivity due to anisotropy variations. At the same time the aspect ratio increase decreases the sensitivity. At low frequencies there is less noise in the device. The other parameter affecting the noise is the junction area which reduces the noises if the area is larger. The integrated MTJs for sensors decrease the detectivity by suppressing the noises which are frequency dependent. A Wheatstone bridge circuit was used to suppress noise in the TMR sensor. At low frequencies the device shows better detectivity and manageable noise spectral density. A steel bar test shows a low magnetic flux leakage. High sensitivity was observed for various lift-off between 4 cm to 20 cm. Silicon based devices, MgO based devices and Magnetic tunnel junctions (MTJs) were used in renewable energy generation circuits. The MTJ provide radiation tolerant when compared to MTJ circuit. The investigation shows the MTJs performance for different electromagnetic irradiation. The MgO-based MTJ devices under gamma-ray radiation were error tolerant. Various irradiation environments were studied to understand the tolerance of the MTJs. The review presented low energy radiations like *X*-ray and infrared. A fluctuation-dissipation theorem was designed in past to investigate the sensitivity of intrinsic magnetic low-frequency noise (LFN). Magnetic sensitivity linear behavior was studied in the LFN. Various shape anisotropies in MTJ were investigated with magnetization fluctuation. The work reported the performance of MTJs with different dimensions, anisotropies and aspect ratios [19, 20].

3 BACKGROUND METHODOLOGY

The performance of the conventional CMOS circuits can be improved using various devices and technology. The gap between the device fabrication and computing

systems design needs new logics and system. In recent times, spintronic devices were used to improve the performance of CMOS devices. The spintronic magnetic tunnel junction (MTJ) can provide faster execution, low power, and infinite endurance compared to the conventional CMOS circuits. The device is suitable for the design and implementation of memories and logic circuits. The leakage problems in conventional CMOS can be rectified by MTJ hybrids or spintronic device embedded with other devices. In MJT the speed and power can be mainly optimized while supply voltage can be kept the same. In memory and logic circuits the supply voltage and noise margins are important to categorize between various logics.

By using MTJ the reading errors and tolerance can be avoided at the maximum extent with better power consumption. MTJs for switching characteristics due to mixed inputs of STT & Ampere field are shown in Fig. 2.

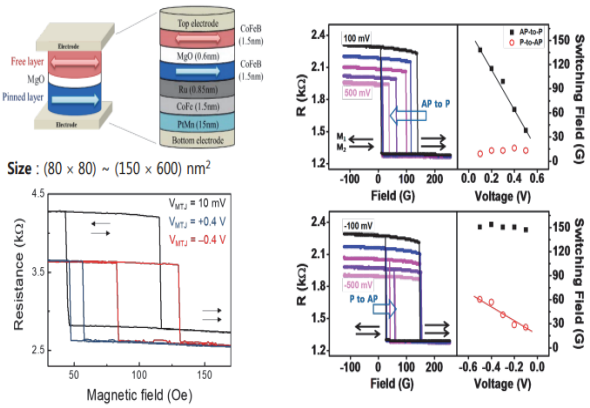

Figure 2 MTJs for switching characteristics due to mixed inputs of STT & Ampere field

Tunnel magneto resistance (TMR) is fabricated in thin film technology and it consists of two ferro magnets separated by a thin insulator where the electrons tunnel from one ferro magnet into the other.

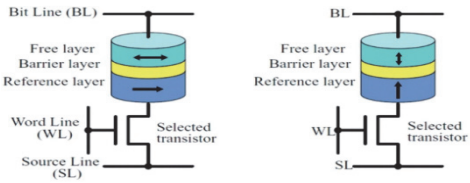

Figure 3 Types of MTJ

Fig. 3 shows the different types of MTJs. The configuration differs in properties like diverse Tunnelling Magnetoresistance Ratio (TMR). The aspect ratio and the magnetic flux gap determine the conduction and the noise immunity. The switching current also depends on the flux gap and the materials. The MgO barrier MTJs have good sensitivity and noise immunity.

The spintronics device uses the spin to store information and thus provides low power, nonvolatility and infinite endurance. It replaced the CMOS device by hybriding with other devices. Especially in memory circuits at deep submicrometer, density is the main requirement and the second order effects due to scaling of CMOS are eliminated. This corresponds to logic 0 and 1. Some disadvantages of the method are the additional hardware requirement and sensing output state initialization is challenging. But with little additional power this can be managed. For the implementation of combinational and sequential memory circuits Penta MTJ is used as shown in Fig. 3. The Penta MTJ-based NAND/NOR and XOR/XNOR logic gates are shown in Fig. 4.

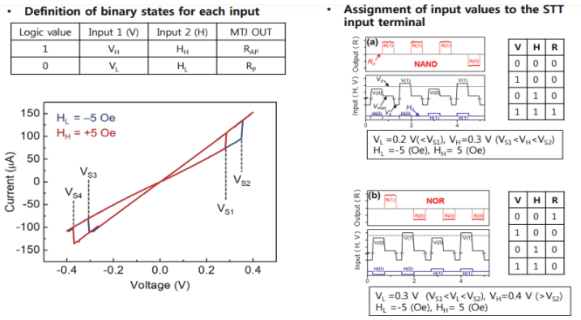

Figure 4 NAND/NOR representation using MTJ

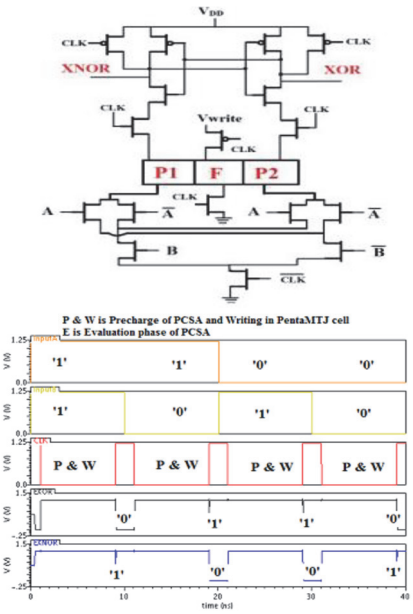

Figure 5 XOR/XNOR gates using Penta MTJ

For designing Sequential logic circuits, since the output depends upon both the previous output (present state) and the present input, the MTJ spin should be considered for the confirmation of the stable output. Since in the sequential circuit like counters where the output differs on only one bit, the total power increases due to the increase in the switching power. In standby condition, conventional CMOS may consume more power when compared to the MTJs. MTJ/Penta MTJ manages the unintentional shutdown and can be restored from the state where the circuit has restarted. The storage device using Penta MTJ is found effective. The restoration rime is only a few picoseconds.

The PentaMTJ, Resistive random access memory (RRAM) and spin-transfer torque magnetic random access memory (STT-MRAM) were based on memristive technologies. These devices are suitable for memory design in system on chip architecture. Spin-transfer torque magnetic random access memories (STT-MRAMs) suffer from current driving capacity. Compared to MTJ, resistive random access memory (RRAM) and phase-change

random access memory (PRAM), MRAM has a low read margin, but is suitable for high density integration like the proposed design in the paper. The proposed design has high endurance. The proposed MTJ also shows CMOS compatibility when compared to the RRAM, STT-MRAM. But the RRAM, STT-MRAM is compatible for embedded application. The proposed design and RRAM, STT-MRAM will be a replacement for SRAM/flash memory, especially for embedded systems and their applications.

4 PROPOSED DESIGN

The proposed FinFET based Penta MTJ-based logic gate block diagram is shown in Fig. 6. The problem of leakage and low voltage swing is avoided. The conventional MTJ headroom problem in pre-charge sense amplifier is avoided. The CMOS Penta MTJ is compatible with other devices so the proposed FINFET process is found efficient in design and no additionnal modeling is required. The CMOS Braun -array and multigate device is implemented using the Short gated FinFET configuration.

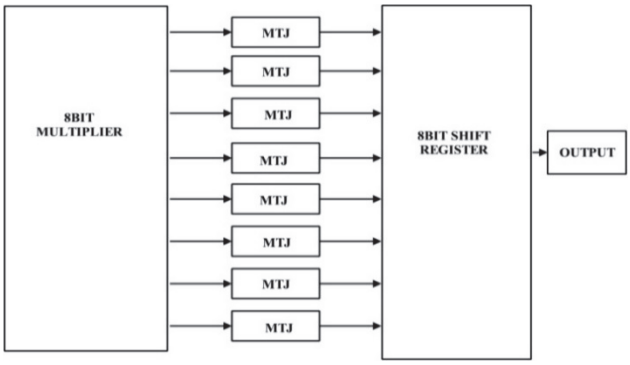

Figure 6 Block diagram of proposed design

The block diagram consists of the 8 bit multiplier, MTJs, 8 bit shift registers and output stage. These multipliers do computation in parallel and combine the partial products. The carry propagation increases the delay and the critical delay of any application circuit decided by the multiplier. Since the idle states are more in CMOS circuits, leakage current increases. But using FinFET MTJ eliminates these problems. Array multiplier is easy to implement so it is used in signal processing application. The circuit is faster but consumes more power. Being used for positive operands based applications Braun algorithm was used for the unsigned binary multiplication.

The Logic gates along with the processing elements form the building blocks of the memory and ALU units. The sensing portion is identical and the proposed design eliminates the errors due to reading. The storage is done at the pinned layers. The parallel stream of MTJ shown in the block diagram supports the information storage. For sequential circuits proper clock circuits are designed. The 'high' output of all logics combines to provide '1' logic while the complement forms the '0' logic. The results are obtained from the shift register as shown in the block diagram. In existing circuit, its worst case delay is proportional to the width of the multiplier. Speed will be slow for very wide multiplier. Once the area is increased, power consumption also increased. The CMOS circuit is affected by second order effects which increases the leakage power.

The advantage of the proposed method is that current driving capability is high. The parallel combination of circuit speeds up the operation in the Braun array parallel multiplier. For Biomedical or DSP applications, the speed of conversion and its computation is important. So parallel array multipliers computing the output of flash ADC is important. This paper does not address the design of flash ADC using FinFET which we kept for future publications. The Braun multiplier with CMOS performs better at high frequency while consuming power in milli range, while for FinFET its performance is very good at frequency range of 600 to 800 MHz. For GHz till 45 nm the power consumption and delay were nominal but at the cost of speed. But using FInFET will improve the design and power consumption. The power dissipation depends on load capacitance, supply voltage, frequency of the clock and total number of switching activities in one clock cycle.

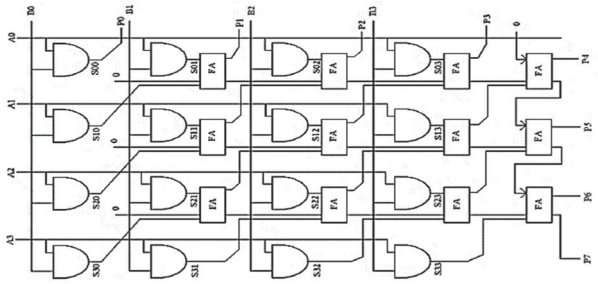

Figure 7 Block diagram of the proposed Braun multiplier using MTJ

The architecture of the Proposed Braun multiplier with MTJ unit to be combined is shown in Fig. 7 The Gates and full adders are implemented in both CMOS, FinFET and FinFET-MTJ. The drawback is that the number of bits increases the component count by which the area and delay increase. The carry propagation in the full adder contributes to the critical delay of the multiplier. By passing transistor may improve the delay but with additional power requirement. Shift registers are required to port the input to the chip and send them to outputs. The clock circuits for input rate are calculated. The schematic diagram of the proposed FinFET design is shown in Fig. 8.

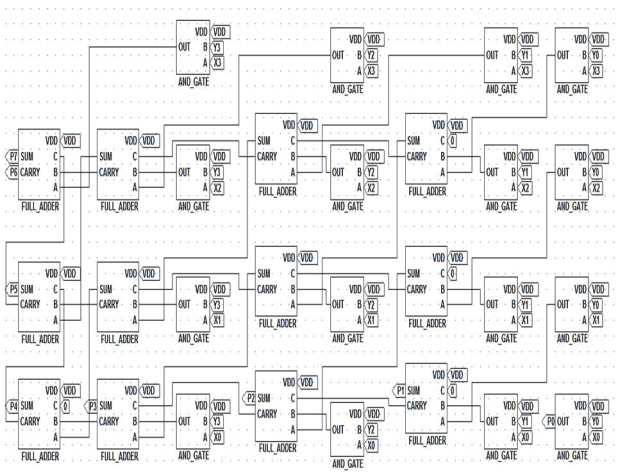

Figure 8 Schematic diagram of proposed finfet based braun multiplier

Ripple Carry adders form the last stage of the multiplier to combine the outputs. FinFET based proposed

design is in the shorted gate configuration. In the independent Gate method, the different gate is given unique voltage levels which are kept for future work and out of scope of this work. The other component in the structure is the fin or Silicon On Insulator (SOI) finger. The fin is protected by silicon fin nitride depositions. The driving capacity of the circuit increases when cascading is applied. In addition the noise margin increases.

5 RESULTS AND DISCUSSION

The circuits are implemented in LTSPICE with predictive technology models. The power calculation and other parameters were taken using Synopsis. The predictive technology models were used. The design was done in 32nm CMOS and FinFET process. The model files define the various parameters like Width, Length, oxide capacitance and threshold voltage. The supply voltage is kept at 1V. The results obtained using SPICE simulations with Predictive Technology Models confirm that the proposed design offers a reliable, high-performance solution for next-generation low-power and high-speed applications. Fig.9 shows the Schematic diagram of array multiplier using MTJ and Fig.10 shows the Schematic diagram of proposed design with MTJ with inputs. The performance is shown in Tab. 1 and Tab. 2.

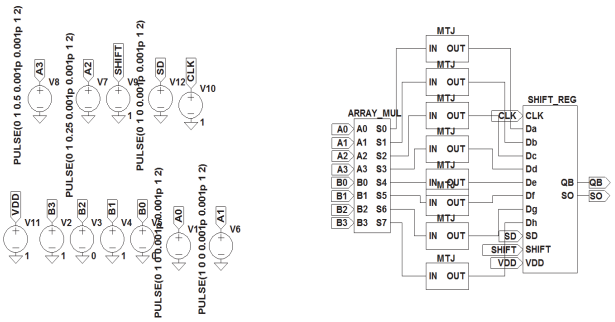

Figure 9 Schematic diagram of array multiplier using MTJ

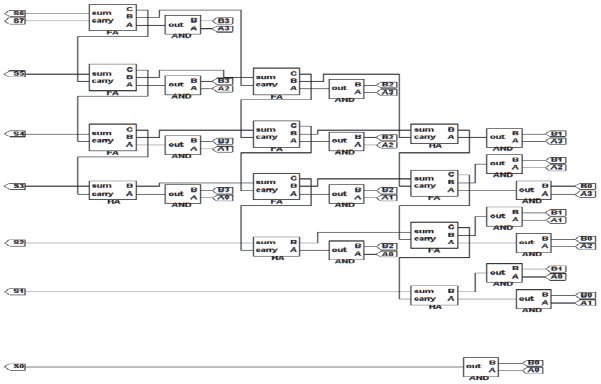

Figure 10 Schematic diagram of proposed circuit (multiplier and shift register cascaded using MTJ)

Tab. 1 shows the power calculation of CMOS and FinFET. The average power of FinFET is less compared to the CMOS average power.

Table 1 Power calculation of CMOS and FinFET (*VDD* = 2 V) *Fin* = 500 MHz

	CMOS / 32 nm				FinFET / 32 nm			
MTJ based design	Average Power / nW	Peak Power / nW	Average Current / nA	Peak Current / nA	Average Power / nW	Peak Power / nW	Average Current /nA	Peak Current / nA
Array Multiplier	7.3	7.7	15.3	16.2	0.62	0.63	1.8	1.4
Proposed	6.7	6.2	14.8	15.5	0.53	0.6	1.3	1.1
Shift register	22.8	23.6	45.2	47.3	4.8	4.7	8.2	8.3
MTJ	31.7	32.3	67.1	68.3	8.1	8.2	15.3	15.3

Table 2 Power calculation of CMOS and FinFET (*VDD* = 1 V) *Fin* = 500 MHz

	CMOS / 32 nm				FinFET / 32 nm			
MTJ based design	Average Power / nW	Peak Power / nW	Average Current /nA	Peak Current / nA	Average Power / nW	Peak Power / nW	Average Current / nA	Peak Current / nA
Array Multiplier	4.2	4.4	4.6	4.7	0.37	0.36	0.29	0.29
Proposed	3.8	3.7	3.7	3.8	0.2	0.2	0.21	0.23
Shift register	11.4	11.8	10.6	10.9	2.4	2.51	2.1	2.3
MTJ	20.5	20.7	43.3	43.6	3.9	3.87	3.4	3.8

Tab. 2 shows the analysis for CMOS and FinFET in *VDD* = 1 V. The power delay product of FinFET is less compared to the CMOS power delay product. The device is better for memory related application but for communication systems like 5G they show moderate performance due to the very high carrier signal usage.

The device is designed in shorted gated mode where the multigate controls the current flowing from the source to drain. The half select problem arrises if there is no gate control. This problem is eliminated in the proposed design. The system is suitable for high computing examples like artificial intelligence architectures. Since the proposed design is suitable for memory based design. AI is the suitable high computing device with more training and testing data. The proposed design is suitable for chips which are designed for high computation logic and arithmetic units

6 CONCLUSION

This paper presents the implementation of a FinFET-based PentaMTJ logic and processing element, demonstrating significant improvements in power consumption and operational accuracy, especially in memory device applications. The design addresses the limitations of conventional CMOS circuits below the 45 nm technology node by leveraging a 32 nm FinFET process, which effectively reduces the area and eliminates

critical issues such as leakage current and switching current fluctuations. The PentaMTJ structure, when implemented in FinFET technology, exhibits superior current driving capability and faster execution compared to conventional CMOS designs. Additionally, the reduced interconnect delay further enhances the overall performance. The results obtained using SPICE simulations with Predictive Technology Models confirm that the proposed design offers a reliable, high-performance solution for next-generation low-power and high-speed applications.

7 REFERENCES

[1] Senthilkumar, V. M., Nirmala, R., Satish Kumar, R., & Vinoth Kumar, K. (2025). Enhanced low power FinFET-based flash ADC design for high-speed electronics applications. *Technical Gazette*, *32*(2), 466-473. https://doi.org/10.17559/TV-20240801001895

[2] Huda, S. & Sheikholeslami, A. (2013). A novel STTMRAM cell with disturbance-free read operation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *60*(6), 1534-1547. https://doi.org/10.1109/TCSI.2012.2220458

[3] Pable, S. D. & Hasan, M. (2012). Interconnect design for subthreshold circuits. *IEEE Transactions on Nanotechnology*, *11*(3), 633-639.

[4] Trinh, H. P., Zhao, W., Klein, J. O., Zhang, Y., Ravelosona, D., & Chappert, C. (2013). Magnetic adder based on racetrack memory. *IEEE Transactions on Circuits and Systems I*: *Regular Papers*, *60*(6), 1469-1477. https://doi.org/10.1109/TCSI.2012.2220507

[5] Rowlands, G. E., et al. (2011). Deep subnanosecond spin torque switching in magnetic tunnel junctions with combined in-plane and perpendicular polarizers. *Applied Physics Letters*, *98*, 102509-3.

[6] Senthilkumar, V. M., Ravindrakumar, S., Nithya, D., & Kousik, N. V. (2019). A Vedic mathematics-based processor core for discrete wavelet transform using FinFET and CNTFET technology for biomedical signal processing. *Microprocessors and Microsystems*, *71*, 102875. https://doi.org/10.1016/j.micpro.2019.102875

[7] Senthilkumar, V. M., Muruganandham, A., Ravindrakumar, S., & Gowri Ganesh, N. S. (2019). FINFET operational amplifier with low offset noise and high immunity to electromagnetic interference. *Microprocessors and Microsystems*, *71*, 102887. https://doi.org/10.1016/j.micpro.2019.102887

[8] Rajaei, R. & Mamaghani, S. B. (2017). Ultra-low power, highly reliable, and nonvolatile hybrid MTJ/CMOS-based full-adder for future VLSI design. *IEEE Transactions on Device and Materials Reliability*. https://doi.org/10.1109/TDMR.2016.2644721

[9] Rajaei, R. (2017). A reliable, low-power, and nonvolatile MTJ-based flip-flop for advanced nanoelectronics. *Journal of Circuits, Systems, and Computers*, *27*(13). https://doi.org/10.1142/S0218126618502055

[10] Gupta, M. K. & Hasan, M. (2016). A low-power robust easily cascaded PentaMTJ-based combinational and sequential circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *24*(1), 218-222. https://doi.org/10.1109/TVLSI.2015.2398117

[11] Polyakov, O., Kuznetsov, V., Shcherbinin, S., Lelikov, E., & Smirnov, A. (2021). Development and research of a theoretical model of the magnetic tunnel junction. *Sensors*, *21*(6), 2118. https://doi.org/10.3390/s21062118

[12] Mohd Noor Sam, M. A. I., Jin, Z., Oogane, M., & Ando, Y. (2019). Investigation of a magnetic tunnel junction-based sensor for the detection of defects in reinforced concrete at high lift-off. *Sensors*, *19*(18), 4718.

[13] Kato, D., Kan, T., Yamada, S., Yakushiji, K., Fukushima, A., & Yuasa, S. (2013). Fabrication of magnetic tunnel junctions with amorphous CoFeSiB ferromagnetic electrode for magnetic field sensor devices. *Applied Physics Express*, *6*, 063001. https://doi.org/10.1143/APEX.6.063001

[14] Cardoso, S., Leitao, D. C., Ferreira, R., Cardoso, F. A., Freitas, P. P., & Martins, V. C. (2014). Magnetic tunnel junction sensors with pTesla sensitivity. *Microsystem Technologies*, *20*, 793-802. https://doi.org/10.1007/s00542-013-2035-1

[15] Fujiwara, K., Nakatani, M., Sato, K., Nakajima, H., Yoshida, S., Enpuku, K., & Sugita, Y. (2018). Magnetocardiography and magnetoencephalography measurements at room temperature using tunnel magneto-resistance sensors. *Applied Physics Express*, *11*, 023002. https://doi.org/10.7567/APEX.11.023001

[16] Hu, J., Luo, W., Sun, X., Wu, H., Liu, X., Li, X., & Zhang, H. (2019). Double-gap magnetic flux concentrator design for high-sensitivity magnetic tunnel junction sensors. *Sensors*, *19*(20), 4475. https://doi.org/10.3390/s19204475

[17] Jin, Z., Oogane, M., Ando, Y., Naganuma, H., & Mizukami, S. (2020). Detection of small magnetic fields using serial magnetic tunnel junctions with various geometrical characteristics. *Sensors*, *20*(2), 5704.

[18] Jin, Z., Oogane, M., Ando, Y., Miwa, S., Naganuma, H., & Mizukami, S. (2021). Serial MTJ-based TMR sensors in bridge configuration for detection of fractured steel bar in magnetic flux leakage testing. *Sensors*, *21*(2), 668. https://doi.org/10.3390/s21020668

[19] Seifu, D., Shrestha, S., Alghamdi, R. A., & Alemayehu, S. (2023). Electromagnetic radiation effects on MgO-based magnetic tunnel junctions: A review. *Molecules*, *28*(10), 4151. https://doi.org/10.3390/molecules28104151

[20] Li, X., Li, Y., Li, J., Zhang, S., Wang, X., Zhou, Y., Zhao, Z., & Zhao, W. (2020). Tunable magnetic low-frequency noise in magnetic tunnel junctions: Effect of shape anisotropy. *Journal of Physics: Condensed Matter*, *32*(49). https://doi.org/10.1088/1361-648X/abb443

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