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Original scientific paper

A High-Performance Fully Differential Low Noise Trans-Impedance Amplifier for Near Infra-Red Spectroscopic Systems

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Abstract: A Fully Differential Low Noise Trans-Impedance Amplifier (FDLN-TIA) with a high Common-Mode Rejection Ratio (CMRR) and Power-Supply Rejection Ratio (PSRR) is proposed for Near Infra-Red Spectroscopic (NIRS) systems. These systems require highly sensitive and precise circuits to detect ultra-low input currents effectively. The presented TIA is designed using a two-stage architecture to achieve a maximum Trans-Impedance Gain (TIG) of 193.24 dBΩ, ensuring accurate signal amplification. The amplifier demonstrates an impressive -3 dB bandwidth of 38.71 MHz, making it suitable for high-frequency applications. The proposed TIA efficiently senses and amplifies ultra-low input currents ranging from 100 pA to 200 pA. A novel modified fully differential amplifier architecture is introduced to achieve low noise performance, enabling effective noise cancellation. A Common Mode Feedback (CMFB) circuit and a power supply noise filter are integrated to improve the CMRR and PSRR, measured at 88.27 dB and 76.35 dB, respectively. The amplifier exhibits an input referred noise current of 0.95 fA/√Hz and an output noise voltage of 1.72 pV/√Hz, contributing to a Signal-to-Noise Ratio (SNR) of 237 dB at 38.71 MHz. The Figure of Merit (FoM) is calculated to be 4.76×10^{35}, highlighting the amplifier's efficiency. Operating from a 1 V supply voltage, the TIA consumes only 8.31 μW power at 27 °C, demonstrating its low-power characteristics. Post-layout simulations confirm the amplifier's performance, and the compact layout, measuring 61.29 μm × 60.61 μm in 45 nm CMOS technology, makes it suitable for integration into modern NIRS systems. This design is a promising solution for enhancing the sensitivity and reliability of NIRS applications with the best noise cancellation.

Keywords: CMOS technology; fully differential amplifier; noise cancellation; Near Infra-Red Spectroscopy (NIRS); trans-impedance gain

1 INTRODUCTION

Trans impedance amplifiers (TIAs) play a crucial role in converting weak signals from photodiodes (PDs) into output voltages, enabling their use in diverse applications, including biosensing and optical communication systems. Recent advancements in bioelectronics and the ease of downsizing electronic biosensors have made TIAs an excellent candidate for diagnosis and detection systems, particularly in wearable and implantable medical devices. Biosensors integrated with TIAs are widely employed in monitoring blood glucose levels for diabetes patients due to their compact size, low power consumption, and high sensitivity. These features necessitate sensitive readout circuitry capable of amplifying ultra-low signals while minimizing noise.

Applications of TIAs span various domains, including optical receivers [1-5].

MEMS sensor readout circuits [6-8], Light Detection and Ranging (LiDAR) systems [9], magnetic resonance imaging (MRI) systems [10], and ultrasound imaging [11-14]. Capacitive-feedback TIA topologies have been implemented to achieve low-noise CMOS front-end amplifiers for interfacing with biosensor arrays in biosensing [15]. Moreover, TIAs are utilized for DNA Sequencing [16], neural recording [17], and reconfigurable TIA designs have been employed in Near Infrared Spectroscopy (NIRS) acquisition [18].

Low-noise cascode TIAs have been developed to achieve large gain and bandwidth [19] for noise-sensitive applications such as Optical Time-Domain Reflectometry (OTDR) [20]. TIAs are used in other generic Biosensing circuits [21], Low-Power Photoplethysmogram Acquisition (PPG) Integrated Circuit [22]. The performance parameters of these TIAs are analyzed.

This paper proposes a fully differential low-noise TIA with a novel architecture tailored for noise-sensitive biosensing applications. The first stage employs an inverter TIA with a very low gain to avoid amplifying noise along with the input signal. The second stage utilizes a modified fully differential amplifier to amplify the output from the first stage while canceling out common-mode noise, achieving a high Common-Mode Rejection Ratio (CMRR). Additionally, a power supply noise filter with high Power-Supply Rejection Ratio (PSRR) enhances the Signal-to-Noise Ratio (SNR).

The paper is structured as follows: Section 2 discusses the limitations of existing Multi-Stage Cascode Common Source (MSCCS) low-noise TIA architectures. Section 3 introduces the proposed novel fully differential low-noise TIA design. Section 4 presents post-layout simulation results and detailed analysis. The conclusion and future directions are provided in Section 5.

2 RELATED WORKS

The existing TIA is a multi-stage cascode-common source (MSCCS)design that achieves a trans-impedance gain of 172 GΩ (184.71 dBΩ) and a bandwidth of 180 kHz with a considerable amount of low noise parameters. The existing low-noise MSCCS TIA has an inverter cascode amplifier in the first-stage and a source follower in the second-stage along with necessary biasing circuits. MSCCS TIA circuit is shown in Fig.1. Various types of amplifiers are used for the implementation of an MSCCS-TIA, including biasing, source-follower, and cascode stages. Cascoding is the technique that combines common-source and common-gate configurations, and greatly increases gain and bandwidth performance when compared to common-source topology. MSCCS-TIA is implemented with reduced noise, increased gain, and low-power dissipation [23]. A low noise amplifier with the preamplifier stage was proposed in this architecture [24]. A trans-impedance amplifier (TIA) is used after a current preamplification stage with a 100 × current gain to achieve a total trans-impedance gain of 160 dB. The read-out circuit uses a 1.8 V supply to consume 5.6 mW and is designed in a 0.18 μm CMOS technology. For cardiac

electrical impedance tomography applications, a wide bandwidth amplifier is introduced in this architecture [25]. A balanced, symmetric architecture without systematic offset was used to reduce mismatch. The performance of the suggested amplifier was demonstrated by designing and fabricating a prototype chip using a 180 nm CMOS technology. The amplifier reduces common-mode interference by operating within a 6 MHz bandwidth. Though the current preamplification architecture [24] exhibits a trans-impedance gain of 160 dBΩ, the power consumption of 5.6 mW is huge and it can heat the chip within a short span. This TIA cannot be used for low-power battery-operated applications. However, the balanced symmetric architecture [25] exhibits a wide bandwidth but the trans-impedance gain of 70 dBΩ is very low. This TIA cannot be used for amplifying very weak photocurrents.

MSCCS-TIA [23] and current preamplification TIA [24] are single-ended amplifiers, so noise cancellation is not possible in this architecture but a small amount of noise reduction is possible. Single-ended amplifiers will amplify the noise also along with the input signal. Moreover, the noise-sensitive biosensors require high CMRR to cancel out the offset voltage and noise present in the input and output signals. It also requires high PSRR to remove power supply noises from the output signal of the TIA.

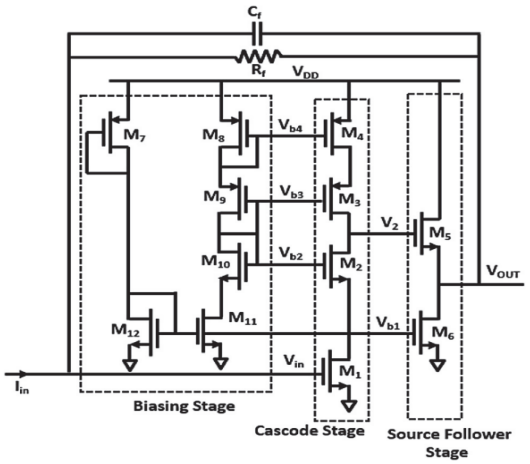

Figure 1 MSCCS TIA [23]

3 PROPOSED METHOD

The proposed TIA is a two-stage amplifier. Stage 1 is an inverter TIA with moderate gain to reduce the noise c from the Inverter TIA. This inverter TIA converts the current signal from the photo-diode into a proportional voltage signal to the second-stage amplifier. The first stage's gain is kept moderate to avoid noise amplification by the first stage. The proposed modified fully differential and fully balanced low-noise TIA with high CMRR and PSRR is implemented in this paper. It has a Common-Mode Feed-Back circuit to provide high CMRR that rejects or eliminates most of the noises present in the input signal and the offset voltages from the amplifier. A power supply noise rejection circuit is implemented to remove the noises coming from the power supply which improves the PSRR value of the FDLN-TIA.

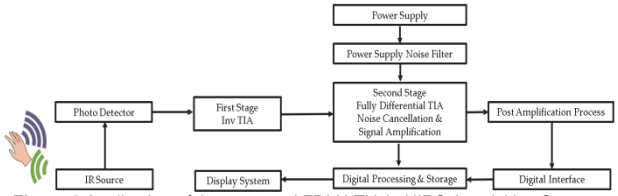

Figure 2 Application of the proposed FDLN-TIA in NIRS Acquisition System

The application of the proposed FDLA-TIA in the NIRS Acquisition System is shown in Fig. 2. The IR resource received from the IR source is reflected by the hand and it is detected by photodetector. The detected signal is amplified by the proposed first-stage Inv TIA and second-stage Fully differential amplifier. Noise cancellation is performed in the second stage and the pre-amplified signal is further amplified by the fully differential amplifier without noise. The amplified signal is converted into digital data for further processing and storage. The power supply noise is removed by the power supply noise filter to improve the overall signal quality.

The schematic diagram of the modified FDLN-TIA is illustrated in Fig. 3. The first stage is implemented using Inverter TIA with the feedback-resistor R_F and feedback capacitors C_{gdp1} & C_{gdn1} (parasitic capacitors). The output signals of the Inverter TIAs V_X^+ and V_X^- are connected to V_{in}^+ and V_{in}^- input terminals of the FDA as shown in the schematic. The amplified signal from the modified fully differential amplifier is measured from the output terminals V_{out}^+ and V_{out}^-. The proposed amplifier design is intended for 100 pA to 200 pA current range only. However, this amplifier architecture can be slightly modified for programmable trans-impedance gain and programmable bandwidth to support a wide range of input currents.

Input differential pair is implemented using M_{P3} and M_{P4} using pMoS transistors with the W/L ratio of 100 µm/1 µm (large width) and the load transistors are implemented using M_{n3} and M_{n4} with the W/L ratio of 1 µm/ 20 µm (long channel length). Transistors M_{n3} and M_{n5} form the current mirror for the left arm and transistors M_{n4} and M_{n6} form the current mirror for the right arm of the modified FDA. The biasing-current of the transistors M_{P7} and M_{P8} is controlled by common-mode-voltage V_{CM}. The differential pair uses very wide pMoS transistors as input transistors to diminish the input-referred-noise current. The load transistors are longer transistors with less width. The necessary bias circuit for the FDA is implemented using pMoS transistors to minimize the noise contributions. The pMoS transistors contribute less noise compared to the nMoS transistors. Hence, the proposed FDLN-TIA circuit is implemented using pMoS differential pair.

The main benefit of a Common-Mode Feedback (CMFB) circuit is its ability to accurately regulate a differential amplifier's common-mode voltage. By actively correcting any deviations from the intended common-mode level, CMFB circuits can greatly increase the circuit's Common-Mode Rejection Ratio (CMRR). The CMFB circuit is implemented using two unity gain amplifiers and two resistors R_1 and R_2. The R_1 and R_2 resistors are of equal values and they are well-matched in the layout to minimize the process variation and the mismatch.

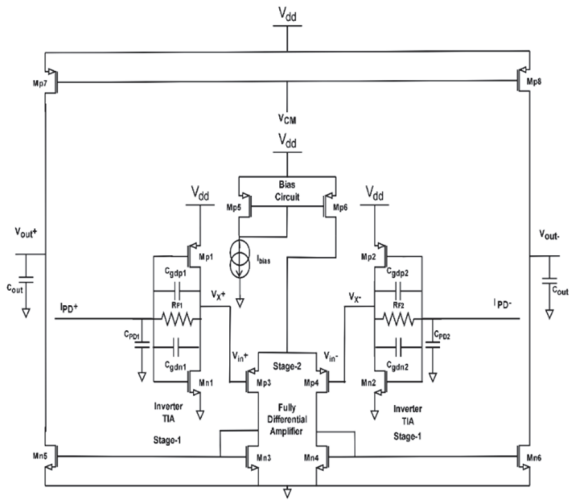

Figure 3 Schematic of the FDLN-TIA

The output signal of the CMFB circuit is denoted as V_{CM} (Common-Mode-Voltage) which is wired to the V_{CM}. The proposed CMFB circuit provides V_{CM} = 0.5 V across all PVT corners. It gives a high Common Mode Rejection Ratio (CMRR) to reject or remove all variations between both arms of the fully differential amplifier. The CMBF schematic is depicted in Fig. 4. The proposed CMFB utilizes two unity gain buffers to provide the best isolation between the CMFB circuit and the amplifier. Since the CMFB circuit is perfectly balanced in the layout also, it provides an accurate common mode voltageof 0.5 V. This gives the differential amplifier a high CMRR by eliminating all undesired noises and spikes.

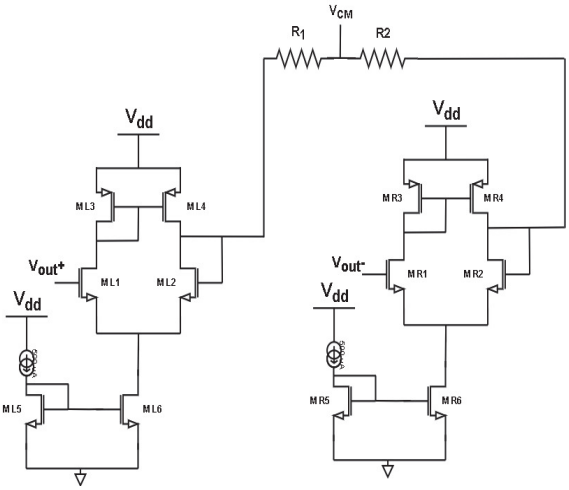

Figure 4 Schematic Diagram of the Common-Mode-Feed-Back (CMFB)

The power supply noise filter is implemented using a 'π' architecture. The capacitors are of equal value. The cutoff frequency is $1/2\pi\sqrt{LC}$. The power supply filter is implemented off the chip because the big inductor and capacitors cannot be fabricated inside the chip. The power supply noise filter is demonstrated in Fig. 5. The power supply noise filter removes all ripples in the output and any supply variations from the V_{dd} and thus provides a high PSRR to the proposed FDLN-TIA. The main benefit of a power supply noise filter is that it greatly lowers electrical noise and ripple on the power supply output, guaranteeing a clean and steady voltage for connected devices, improved performance and signal quality. By removing undesired electrical noise spikes and harmonics, a power supply noise filter also helps to minimize interferences.

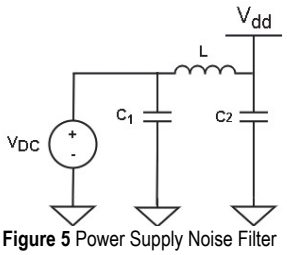

Figure 5 Power Supply Noise Filter

The input differential pair and the bias circuit use pMoS transistors to minimize the noise contributions by these transistors. The overall noise is reduced by the proposed FDLN-TIA. Hence, the output noise voltage and the input noise current are very low in the proposed FDLN-TIA. The transistor sizing is listed in Tab. 1 and the component values are exhibited in Tab. 2. and Tab. 1 illustrates that the input differential pair uses wider pMoS transistors (M_{P3} and M_{P4}), longer nMOS transistors ($M_{n3} - M_{n6}$) as load to minimize the noise contribution by the input and load transistors.

Table 1 Transistor Dimension

Transistors	W / μm/	L / μm
M_{n1}	10	1
M_{n2}	10	1
M_{n3}	1	20
M_{n4}	1	20
M_{n5}	1	20
M_{n6}	1	20
M_{p1}	20	1
M_{p2}	20	1
M_{p3}	100	1
M_{p4}	100	1
M_{p5}	2	4
M_{p6}	8	4
M_{p7}	4	10
M_{p8}	4	10

The passive component values were chosen to minimize the noise contributed by them. Input Photo-Diode capacitance is 1nF and the output load capacitor is 1 pF. A very small capacitor in Femto-Farads is selected as a photo-diode capacitor to minimize the noise contributed by the photo-diode capacitor. Since the input capacitor is huge compared to the load capacitor, the dominant pole is contributed by the input capacitor. The input capacitor plays a major role in bandwidth calculation.

Table 2 Passive Components Value

Component	Value
$C_{PD1} = C_{PD2}$	1 nF
C_{out}	1 pF
$C_{gdp1} = C_{gdp1} = C_{gdn1} = C_{gdn1}$	1 fF
R_F	100 MΩ
I_{PD}	100 pA
L	100 nH
C_1	1 μF
C_2	1 μF

3.1 Circuit Analysis

The first stage is the inverter trans-impedance amplifier and its open-loop trans-impedance gain and the

open-loop output-resistance are denoted by A_{Inv} and R_{out} respectively. The transconductance of the transistor is computed by Eq. (2) and the drain current is calculated by Eq. (3).

$$A_{VOL1} = A_{Inv} = -G_m \times R_{out} = -\left(g_{mn1} + g_{mp1}\right) \times R_{\text{out}} \tag{1}$$

$$Transconduc\,tan\,ce\left(g_m\right) = \sqrt{\mu_n x C_{0x} x \left(W / L\right) \times I_D} \tag{2}$$

$$Drain\ Current\left(I_D\right) = \left(1/2\right) \times \mu_n \times C_{0x} \times \times \left(W / L\right) \times \left(V_{gs} - V_{th}\right)^2 \tag{3}$$

By applying the values of the electron's mobility (μ_n), Gate capacitance (Cox), transistor's Width (W), transistor's Length (L) and the drain-current (I_D) of the transistors, the transconductance is calculated. The output-resistance of the inverter TIA is calculated by the Eq. (4).

$$R_{out} = r_{op1} \times \| \times r_{on1} \tag{4}$$

where r_{on1} and r_{op1} are the drain-source resistances of M_{n1} and M_{p1} respectively and R_F is the feedback-resistor of the first-stage Inv_TIA. C_{in} is the net input-capacitance consisting of the miller capacitance and the Photo-Diode (PD) junction-capacitance due to C_{gdn1} and C_{gdp1} denoted by Eq. (5).

$$C_{in} = C_{PD} + \left(C_{gdn1} + C_{gdp1}\right)\left(\left|A_{Inv}\right| + 1\right) \tag{5}$$

The zero-frequency input-impedance is derived based on the feedback theory by Eq. (6).

$$Z\left(0\right)_{in} = \frac{R_{\text{out}} + R_F}{-G_m R_{\text{out}} + 1} \tag{6}$$

The input-pole is the dominant-pole when C_{in} is huge compared to C_{out}, and the bandwidth is derived by the Eq. (7).

$$Bandwidth = \frac{G_m R_{\text{out}} + 1}{2\pi\left(R_{\text{out}} + R_F\right) C_{\text{in}}} \tag{7}$$

Inverted TIA's closed-loop gain is calculated by Eq. (8)

$$A_{VCL1} = \frac{v_x}{I_{in}} = A_{VOL} \frac{Z_F}{1 - A_{VOL}} \tag{8}$$

Since, $A_{VOL} = A_{Inv}$.

Inverted TIA's closed-loop gain is calculated by Eq. (9).

$$A_{VCL1} = A_{Inv} \frac{Z_F}{1 - A_{Inv}} \tag{9}$$

$$Z_F = \frac{R_F}{1 + R_F C_F s} \tag{10}$$

The feedback capacitor C_F of the first stage is calculated by the Eq. (11).

$$C_F = C_{gdp1} + C_{gdn1} \tag{11}$$

The second stage is a fully-differential-amplifier and the open-loop-gain is calculated by Eq. (12), where g_{mp3} is the transconductance and r_{o3} and r_{o5} are the output-resistance of the transistors M_{n3} and M_{n5} respectively.

$$A_{Diff} = -g_{mp3}\left(r_{on3} \| r_{on5}\right) \tag{12}$$

The total-gain of the FDLN-TIA is computed by the Eq. (13).

$$A_{V\_Total} = A_{VCL1} A_{Diff} \tag{13}$$

$$A_{V\_Total} = A_{Inv} \frac{Z_F}{1 - A_{Inv}} \times g_{mp3}\left(r_{on3} \| r_{on5}\right) \tag{14}$$

$$A_{V\_Total} = A_{Inv} \frac{R_F}{\left(1 + R_F C_F s\right)\left(1 - A_{Inv}\right)} \times \times g_{mp3}\left(r_{on3} \| r_{on5}\right) \tag{15}$$

The open loop input-impedance of the first-stage Inverter TIA is calculated by Eq. (16).

$$Z_{in} = \frac{V_{\text{in}}}{I_{\text{in}}} \tag{16}$$

The open-loop output-impedance of the second-stage is calculated by Eq. (17)

$$Z_{\text{out}} = \frac{V_{\text{out}}}{I_{\text{out}}} = \left(r_{on3} \| r_{on5}\right) \tag{17}$$

Inverter TIA's closed loop input-impedance is calculated by Eq. (18)

$$Z_{\text{in}CL1} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{Z_F}{1 - A_{VOL}} = \frac{R_F}{\left(1 + R_F C_F s\right)\left(1 - A_{Inv}\right)} \tag{18}$$

Common-Mode-Rejection-Ratio (CMRR) is the ratio between differential gain and common-mode-gain. It is represented by the Eq. (19).

$$CMRR = \frac{A_{Diff}}{A_{Com}} \tag{19}$$

CMRR is expressed as decibels by the Eq. (20).

$$CMRR = 20\log_{10}\left[\frac{A_{Diff}}{A_{Com}}\right] \tag{20}$$

CMRR is measured in positive decibels, and a higher CMRR provides better noise rejection. This is because differential gain should be greater than common-mode gain, so the result will be a positive number. CMRR is an important specification that indicates how much common-mode signal is allowed in the output. Common-mode voltages can be in the form of noise or a DC bias from a previous signal stage. CMRR is frequently crucial for mitigating transmission line noise, and its value can depend on signal frequency. For example, a perfect differential amplifier has a CMRR of infinity because A_{Com} is zero in an ideal differential amplifier. The proposed TIA exhibits a CMRR of 88.27 dB.

Power-Supply-Rejection-Ratio (PSRR) is defined as the ratio between variation in input voltage and corresponding variation in the output voltage that is represented in the Eq. (21).

$$PSRR = \frac{\Delta V_{\text{in}}}{\Delta V_{\text{out}}} \tag{21}$$

PSRR can also be expressed as decibels by Eq. (22).

$$PSRR = 20\log_{10}\left[\frac{\Delta V_{\text{in}}}{\Delta V_{\text{out}}}\right] \tag{22}$$

The proposed TIA exhibits a PSRR of 76.35 dB.

The Signal to Noise Ratio SNR is defined as the ratio between signal voltage and noise voltage which is measured in decibels (dB). It is represented by the Eq. (23).

$$\begin{aligned} &Signal\ to\ Noise\ Ratio\ \left(SNR\right) = \\ &= 20\log_{10}\left[\frac{Output\ Signal\ Voltage}{Output\ Noise\ Voltage}\right] \end{aligned} \tag{23}$$

This TIA exhibits the SNR of 237 dB at 38.71 MHz which is a -3dB Bandwidth of the TIA.

The Figure-of-Merit is calculated by Eq. (24).

$$\begin{aligned} &Figure\ of\ Merit\left(FoM\right) = \\ &= \frac{Gain\left(dB\Omega\right)\times Bandwidth\left(MHz\right)}{Power\left(mW\right)\times Input\ Noise\ Current\ \left(fA/\sqrt{Hz}\right)} \end{aligned} \tag{24}$$

3.2 Noise Analysis

FDLN-TIA's noise-model is exhibited in Fig. 6. Noise-current of the MoSFET has two parts: they are flicker noise and thermal noise. Flicker noise is predominantly present in the low-frequency band whereas thermal noise is seen in the high-frequency band. The noise current is modelled as a current-source connected between the drain and source terminals of the MoSFET. MoSFET's input-noise-current is represented by Eq. (25).

$$I_{nt,nf}^2 = 4kT\gamma g_m + \frac{Kf}{C_{ox}W.L.f}\times g_m^2 \tag{25}$$

The thermal-noise contribution by feedback-resistor is denoted by Eq. (26).

$$I_{nt,R_F}^2 = \frac{4kT}{R_F} \tag{26}$$

where k = 1.3807910 - 23 J/K is the Boltzmann constant, T is temperature, g_m is the transconductance, K_f is a process constant, C_{ox} is the gate-oxide, W is the channel width, L is the channel length, 'f' is the frequency, 'γ' is the excess noise factor of the transistor in the strong-inversion region and R_F is the feedback resistance. In Eq. (25), the first-term is the thermal noise and the second-term is the flicker noise. In Eq. (25), the subscripts "*nf*" and "*nt*" represent the flicker-noise and thermal-noise, respectively.

The thermal-noise contributed by the feedback resistors R_{F1} and R_{F2} is cancelled by each other by the fully-differential amplifier since the values of the R_{F1} and R_{F2} are exactly equal and the noise has opposite phases. A very good matching is provided in the layout by the common centroid layout matching technique to minimize the mismatches in the Montecarlo simulations.

The noise sources are modelled as a current-source from source to drain in Fig 6. The nMoS noise-current sources (M_{n1}, M_{n2}, M_{n3}, M_{n4}, M_{n5}, M_{n6}) are highlighted in blue color and the pMoS noise sources (M_{p1}, M_{p2}, M_{p3}, M_{p4}, M_{p6}, M_{p7}, M_{p8}) are highlighted in red color. The total noise contributed by all the MoSFETs and the feedback resistors is expressed in Eq. (27). The total input-referred noise-current contributed by all nMoS and pMoS transistors can be calculated by substituting the values of the device parameters in the Eq. (28). The total-noise contribution can be measured from noise analysis using noise simulation in Cadence Virtuoso using Spectre simulator.

$$\begin{aligned} I_{nt,nfTotal}^2 &= I_{nt,nf\_n1}^2 + I_{nt,nf\_n2}^2 + I_{nt,nf3} + \\ &+ I_{nt,nf\_n4}^2 + I_{nt,nf5} + I_{nt,nf\_n6}^2 + I_{nt,nf\_p1}^2 + \\ &+ I_{nt,nf\_p2}^2 + I_{nt,nf\_p3}^2 + I_{nt,nf\_p4}^2 + I_{nt,nf\_p6}^2 + \\ &+ I_{nt,nf\_p7}^2 + I_{nt,nf\_p8}^2 + I_{nt,nf\_R_{F1}}^2 + I_{nt,nf\_R_{F2}}^2 \end{aligned} \tag{27}$$

$$I^2_{nt,nf\_Total} = 4kTy\left[g_{mn1}+g_{mn2}+g_{mn3}+g_{mn4}+ +g_{mn5}+g_{mn6}+g_{mn1}+g_{mn2}+g_{mn3}\times+g_{mn4}+g_{mn6}+ +g_{mn7}+g_{mn8}\right]+\frac{K_f}{C_{ox}\times f}\times\left[\frac{g^2_{mn1}}{W_{n1}\times L_{n1}}+\frac{g^2_{mn2}}{W_{n2}\times L_{n2}}+ +\frac{g^2_{mn3}}{W_{n3}\times L_{n3}}+\frac{g^2_{mn4}}{W_{n4}\times L_{n4}}+\frac{g^2_{mn5}}{W_{n5}\times L_{n5}}+\frac{g^2_{mn6}}{W_{n6}\times L_{n6}}+ +\frac{g^2_{mp1}}{W_{p1}\times L_{p1}}+\frac{g^2_{mp2}}{W_{p2}\times L_{p2}}+\frac{g^2_{mp3}}{W_{p3}\times L_{p3}}+\frac{g^2_{mp4}}{W_{p4}\times L_{p4}}+ +\frac{g^2_{mp6}}{W_{p6}\times L_{p6}}+\frac{g^2_{mp7}}{W_{p7}\times L_{p7}}+\frac{g^2_{mp8}}{W_{p8}\times L_{p8}}\right]+ +4kTy\left[\frac{1}{R_{F1}}+\frac{1}{R_{F2}}\right] \quad (28)$$

Similarly, the proposed FDLN-TIA's output-noise voltage is represented by Eq. (29). In Eq. (29), the following terms are exactly equal and with opposite signs due to the differential architecture. Hence, these terms will cancel each other. The final output noise voltage after cancelling all the respective terms can be written as Eq. (30).

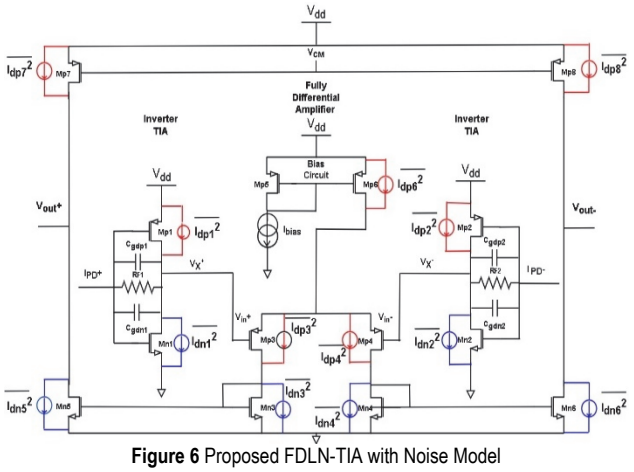

Figure 6 Proposed FDLN-TIA with Noise Model

$$V^2_{nt,nf\_Out} = \frac{I^2_{nt_{n1}}}{g_{mn1}}+\frac{-I^2_{nt_{n2}}}{g_{mn2}}+\frac{-I^2_{nt_{n3}}}{g_{mn3}}+\frac{-I^2_{nt_{n4}}}{g_{mn4}}+\frac{I^2_{nt_{n5}}}{g_{mn5}}+ +\frac{-I^2_{nt_{n6}}}{g_{mn6}}+\frac{I^2_{nt_{p3}}}{g_{mp3}}+\frac{-I^2_{nt_{p4}}}{g_{mp4}}+\frac{I^2_{nt_{p6}}}{g_{mp6}}++\frac{I^2_{nt_{p7}}}{g_{mp7}}+\frac{I^2_{nt_{p8}}}{g_{mp8}}+ +\left[\frac{K_f}{C_{ox}\times f\times W_{n1}\times L_{n1}}+\frac{-K_f}{C_{ox}\times f\times W_{n2}\times L_{n2}}+ +\frac{K_f}{C_{ox}\times f\times W_{n3}\times L_{n3}}+\frac{-K_f}{C_{ox}\times f\times W_{n4}\times L_{n4}}+ +\frac{K_f}{C_{ox}\times f\times W_{n5}\times L_{n5}}+\frac{-K_f}{C_{ox}\times f\times W_{n6}\times L_{n6}}+ +\frac{K_f}{C_{ox}\times f\times W_{p1}\times L_{p1}}+\frac{-K_f}{C_{ox}\times f\times W_{p2}\times L_{p2}}+ +\frac{K_f}{C_{ox}\times f\times W_{p3}\times L_{p3}}+\frac{-K_f}{C_{ox}\times f\times W_{p4}\times L_{p4}}++\frac{K_f}{C_{ox}\times f\times W_{p6}\times L_{p6}}+ +\frac{K_f}{C_{ox}\times f\times W_{p7}\times L_{p7}}++\frac{-K_f}{C_{ox}\times f\times W_{p8}\times L_{p8}}\right] \quad (29)$$

$$\frac{I^2_{nt_{n1}}}{g_{mn1}}=\frac{-I^2_{nt_{n2}}}{g_{mn2}};\frac{I^2_{nt_{n3}}}{g_{mn3}}=\frac{-I^2_{nt_{n4}}}{g_{mn4}};\frac{I^2_{nt5}}{g5}==\frac{-I^2_{nt_{n6}}}{g_{mn6}};\frac{I^2_{nt_{p3}}}{g_{mp3}}= =\frac{-I^2_{nt_{p4}}}{g_{mp4}};\frac{I^2_{nt_{p7}}}{g_{mp7}}==\frac{I^2_{nt_{p8}}}{g_{mp8}};\frac{K_f}{C_{ox}\times f\times W_{n1}\times L_{n1}}= =\frac{-K_f}{C_{ox}\times f\times W_{n2}\times L_{n2}};\frac{K_f}{C_{ox}\times f\times W_{n3}\times L_{n3}}= =\frac{-K_f}{C_{ox}\times f\times W_{n4}\times L_{n4}};\frac{K_f}{C_{ox}\times f\times W_{n5}\times L_{n5}}= =\frac{-K_f}{C_{ox}\times f\times W_{n6}\times L_{n6}};\frac{K_f}{C_{ox}\times f\times W_{p1}\times L_{p1}}= =\frac{-K_f}{C_{ox}\times f\times W_{p2}\times L_{p2}};\frac{K_f}{C_{ox}\times f\times W_{p3}\times L_{p3}}= =\frac{-K_f}{C_{ox}\times f\times W_{p4}\times L_{p4}};\frac{K_f}{C_{ox}\times f\times W_{p7}\times L_{p7}}= =\frac{-K_f}{C_{ox}\times f\times W_{p8}\times L_{p8}}$$

$$V^2_{nt,nf_{\text{Out}}} = \frac{I^2_{nt_{p6}}}{g_{mp6}}+\frac{K_f}{C_{ox}\times f\times W_{p6}\times L_{p6}} \quad (30)$$

In Eq. (30), the first-term is thermal-noise and the second-term is flicker-noise. The output noise voltage is measured from the noise simulations done by using the Cadence Virtuoso and Spectre Simulator with the appropriate simulation setup.

3.3 Noise Cancellation

The proposed modified fully differential amplifier with perfectly matched left arm and right arm is implemented to cancel the noise. The left arm and right arm are perfectly matched in the layout by a common centroid matching technique. Since the dimensions of the MoSFETs M_{P3} & M_{P4} are equal and they are connected to left arm and right arm of the fully differential amplifier respectively, the noise contributions by M_{P3} & M_{P4} will be of equal amount but in the opposite phase to each other. Hence the noise contributions (thermal noise and flicker noise) by M_{P3} will be cancelled out by M_{P4}. Similarly, the noise contribution by M_{P1} and M_{P2}, M_{P7} and M_{P8}, M_{N1} and M_{N2}, M_{N3} and M_{N4}, M_{N5} and M_{N6} and R_{F1} and R_{F2} will cancel out each other. The noise contributions by the CMFB circuit components are not considered. The flicker-noise and the thermal-noise contribution by M_{P6} only will remain in the system and all other noise contributions will be cancelled out by the proposed modified fully differential architecture.

The input-referred noise-current is generally computed by dividing the output-noise voltage from Eq. (30) by the transconductance g_{m3} & g_{m4} and its unit is A/√Hz. Since the M_{P3} & M_{P4} are of the same size, the g_m of both MoSFETs is equal. Hence, the Input-referred-noise-current is computed from the output-noise-voltage by Eq. (31).

$$I^2_{nt,nf_{\text{Total}}} = \frac{V^2_{nt,nf_{\text{Out}}}}{g^2_{mp3}} \quad (31)$$

From Eq. (31), it is evident that the input-referred noise current is directly proportional to the output-noise-voltage and it is inversely-proportional to the square of the transconductance of the input transistors of the differential pair. Hence, the input-referred-noise can be minimized by increasing the transconductance of the differential pair. By combining Eq. (2) and Eq. (32), Eq. (32) can be rewritten as follows and it is denoted as Eq. (32).

$$I^2_{nt,nf_{Total}} = \frac{V^2_{nt,nf_{\text{Out}}}}{\mu_n C_{ox} \times \left(W_{p3} / L_{p3}\right) \times I_D} \tag{32}$$

Optimum sizing is used for the input differential pair (wider transistors with high g_m) and the load transistors (longer transistors with low g_m) to minimize the noise contribution (thermal noise and flicker noise) from these active devices. The input differential pair and the current mirrors use wide pMoS transistors to minimize the noise contributions.

4 RESULTS AND DISCUSSIONS

The proposed FDLN-TIA is implemented in a CMOS 45 nm process node. The post-layout simulations are performed in Cadence Virtuoso. The input and output waveforms of FDLN-TIA are displayed in Fig. 7. The input-current is 100 pA to 200 pA. The input-current is fed to first stage differentially. The first stage is an inverter TIA connected to both arms of the differential-amplifier. The output is in the range of 900 mV. The transfer characteristics of the FDLN-TIA are exhibited in Fig. 7. The input-current is varied from 0 pA to 200 pA to analyze the transfer characteristics. As the input-current is varied, the amplified output varies linearly from 0 mV to 900 mV as shown in Fig. 7.

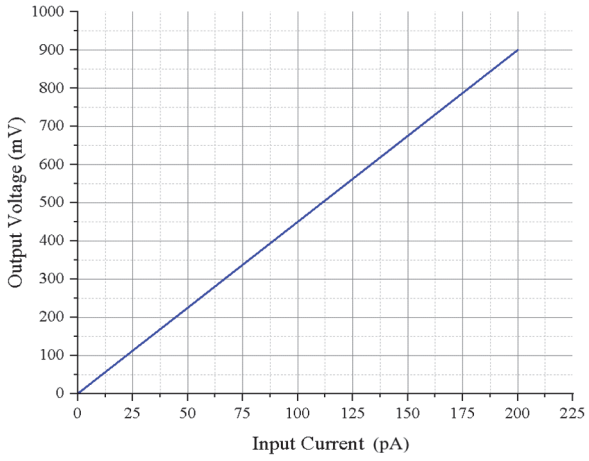

Figure 7 Input Output transfer characteristics of the Fully Differential TIA

Frequency-response of the FDLN-TIA is depicted in Fig. 8. The frequency response is plotted from 1 MHz to 1 GHz. The trans-impedance gain is 193.24 dBΩ and the 3 dB bandwidth is 38.71 MHz. The frequency-response of the input-referred-noise current of the proposed FDLN-TIA is plotted in Fig. 8. From the figure it is evident that the input-referred-noise current is less than 0.95 fA/√Hz from 1 kHz to 38.71 MHz frequency band and it gradually increases after 38.71 MHz as the frequency increases. At the lower band, the flicker noise contribution is higher and is reduced as the frequency increases. Whereas, the thermal noise is less at the lower frequency band. It increases at high frequencies.

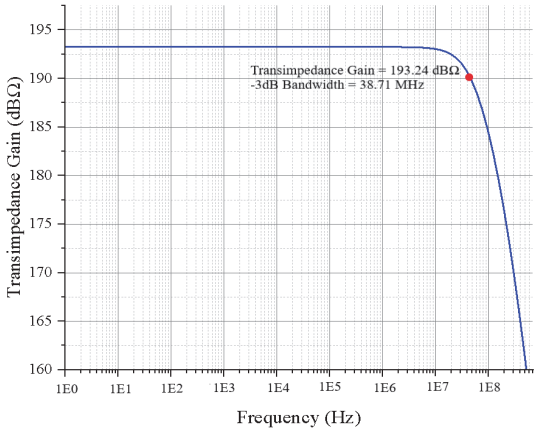

Figure 8 Frequency-response of the Transimpedacne Gain

In the proposed FDLN-TIA, the left-arm and right-arm transistor sizes are exactly equal. Hence, the flicker-noise and thermal-noise contributions from various transistors and resistors are cancelling each other as mentioned in Eq. (30) due to the modified fully differential architecture. The pMoS transistor M_{P6} contributes the remaining noise and it is very low. Hence, the proposed FDLN-TIA exhibits a very-low input-referred noise current of 0.95 fA/√Hz at 38.71 MHz compared to [21-25]. Frequency-response of the output noise voltage is plotted from 1 MHz to 1 GHz frequency range in Fig. 9. The output noise due to flicker noise voltage is high at low-frequency band. As the frequency increases from 1 MHz, the thermal noise starts increasing exponentially from 1 MHz. The maximum output noise voltage is measured at 38.71 MHz which is the −3 dB cutoff frequency. The proposed FDLN-TIA exhibits an output noise voltage of 1.72 pV/√Hz which is very low compared to [21-25] after the noise cancellation.

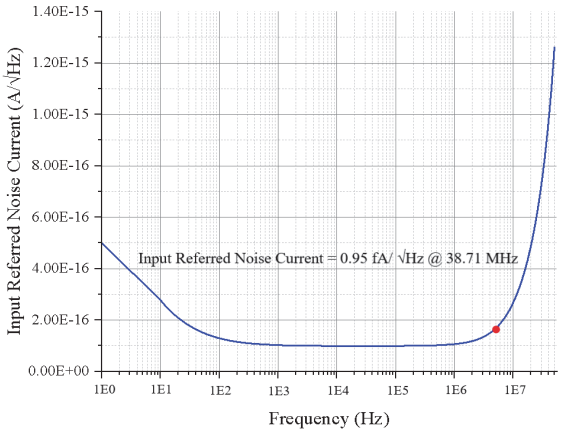

Figure 9 Frequency response of the Input-referred noise-current

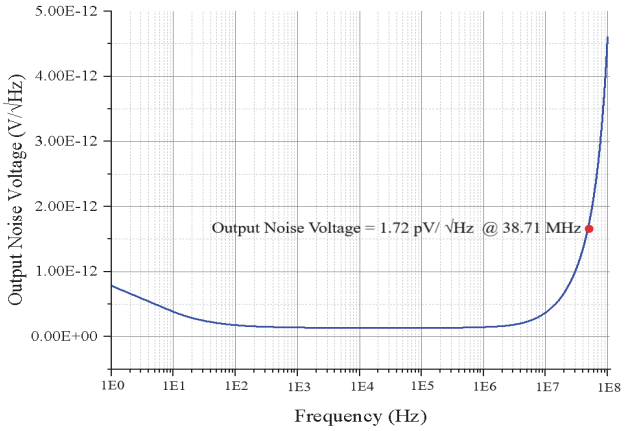

Figure 10 Frequency response of the output noise voltage

Frequency response of the SNR is shown in Fig. 11. SNR is calculated based on the Eq. (23). From Fig. 11, it is evident that the SNR decreases as the frequency increases. The proposed FDLN-TIA exhibits an SNR of 237 dB at −3 dB frequency of 38.71 MHz.

The SNR is inversely proportional to the output-noise-voltage. Since the output-noise-voltage is very low in the FDLN-TIA, the SNR is very high. Since the output SNR is high, the proposed FDLN-TIA provides a better noise performance compared with existing TIAs [21-25] in the literature.

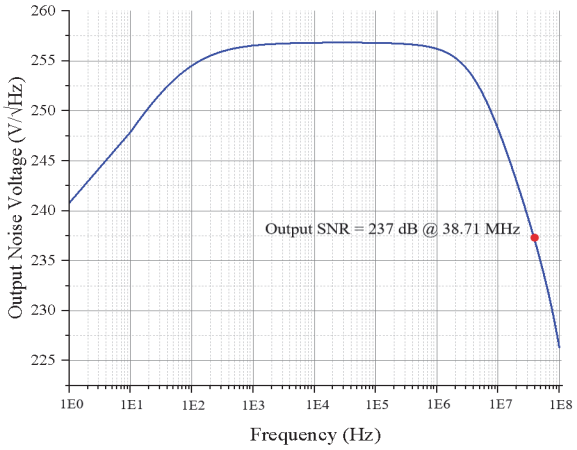

Figure 11 Frequency response of the Output SNR

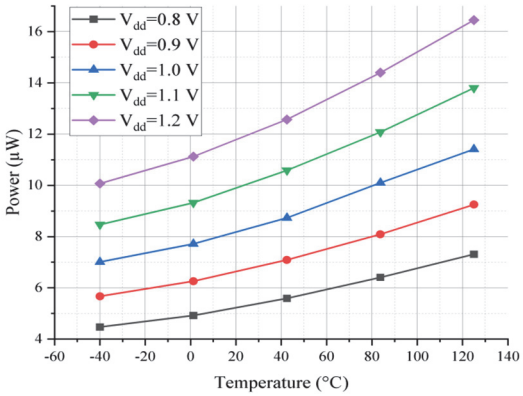

Figure 12 Impact of temperature on the power consumption

The impact of temperature on power consumption for various supply-voltages is displayed in Fig. 12. The simulation is performed from −40 °C to 125 °C which is the industry standard range of temperature. From the graph, it is evident that the power consumption increases exponentially as the Vdd and temperature increase linearly. The proposed FDLN-TIA consumes 8.31 µW power at 27 °C from a 1V supply voltage.

The Monte-Carlo simulation result is shown in Fig. 13. The Monte-Carlo simulation is performed with 100 random samples to analyze the variations in the trans-impedance gain across all Process Voltage Temperature (PVT) corners.

From the simulation results it is evident that the variation is very low. The mean value is 193 dBΩ and the standard deviation is 3.10 dBΩ. The minimum standard deviation shows that the proposed FDLN-TIA provides the mean trans-impedance gain of 193 dBΩ across all PVT corners (Fast-Fast (F-F), Fast-Slow (F-S), Slow-Fast (S-F), Slow-Slow (S-S), Typical (Typ) nMoS and pMoS transistors) and the variation is very minimal due to the best layout matching techniques with optimal transistor sizing.

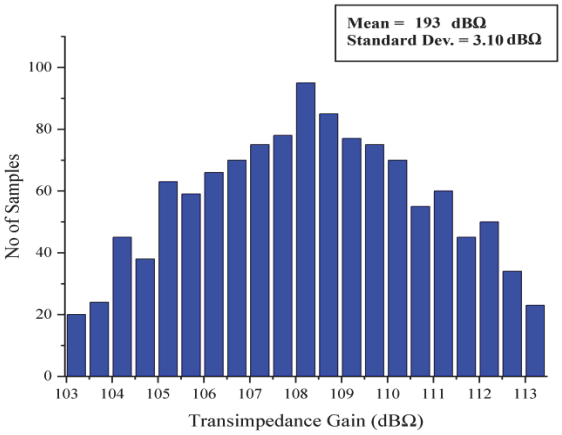

Figure 13 Monte-Carlo Simulation of the trans-impedance gain

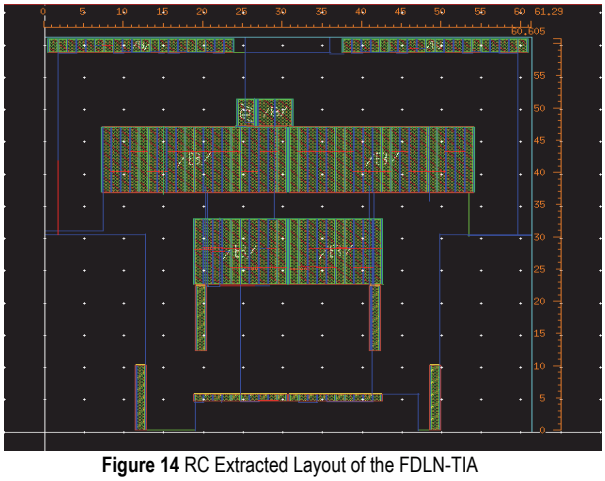

Figure 14 RC Extracted Layout of the FDLN-TIA

The layout diagram of the FDLN-TIA is shown in Fig. 14. Layout occupies an area of 61.29 µm × 60.61 µm. Various layout matching techniques such as common centroid and interdigitation are applied to minimize the coupling capacitors and to maintain the exact symmetricity between the left arm and right arm of the differential amplifier. The proposed layout has minimum parasitic capacitances in the range of a few atto-farads due to a well-matched and optimized layout. A well-matched and optimized layout provides high CMRR for the differential amplifier. High CMMR rejects or removes all common mode variations between V_{out}^{+} and V_{out}^{-} terminals and

provides a noise-free output signal. The noise cancellations by the matching are observed in the post-layout simulations.

This design can be further implemented in the lower technology nodes such as 28 nm and 12 nm etc as a future scope of the work. This amplifier architecture can be slightly modified for programmable trans-impedance gain and programmable bandwidth to support a wide range of input currents. If the photocurrent is in the range of a few hundred picoampers or micro ampers, then the gain of the first and second stages should be minimized to the required output level.

Table 3 Performance Comparison

Description	[25]	[24]	[23]	[22]	[21]	Proposed
Technology (nm)	180	180	180	130	45	45
Trans-Impedance Gain (dBΩ)	9.5	160	184.71	110.88	100	193.24
Bandwidth	6 MHz	1.3 MHz	180 kHz	500 Hz	25 MHz	38.71 MHz
Input Noise Current	-	11 fA/√Hz	18 fA/√Hz	260 pA/√Hz	-	0.95 fA/√Hz
Output Noise Voltage	14.2 nV/√Hz	-	-	-	-	1.72 pV/√Hz
Supply-Voltage / V	3.30	1.80	1.40	1.20	1.0	1.0
Power-Consumption	549 µW	5.6 mW	52µW	26.4 µW	12 µW	8.31 µW
SNR / dB	-	-	-	-	-	237 dB
FoM	1.71×10^{20}	-	3.3×10^{32}	2.53×10^{26}	-	4.76×10^{35}
CMRR / dB	-	-	-	-	-	88.27
PSRR / dB	-	-	-	-	-	76.35
Layout Area	0.058 × 0.058 mm × mm	354 µm × 354 µm	110 µm × 140 µm	NA	0.07 mm × 0.07 mm	61.29 µm × 60.61 µm
Application	Bio-sensor	Bio-sensor	Bio-sensor	Bio-sensor	Bio-sensor	Bio-sensor

The performance parameters of the reported TIAs in the literature [21-25] are compared in Tab. 3. A high-gain TIA was implemented in 45 nm CMOS technology for biosensors with low power dissipation of 12 µW [17]. A low-power photo plethys mogram acquisition integrated circuit was implemented in 130 µm CMOS technology as transimpedance gain of 110.88 dBΩ and 500 Hz bandwidth. This circuit consumes 26.4 µW power from 1.2 V power supply.

A low-noise and low-power multi-stage trans-impedance amplifier for amperometric-based blood glucose monitoring systems was implemented in 180 nm with a transimpedance-gain of 184.71 dBΩ and a bandwidth of 180 KHz. This TIA consumes 52 µW power from 1.4 V power supply [23]. A low noise TIA for the current-readout circuit with 160 dB transimpedance-gain consumes 5.6 mW power from the 1.8 V power supply [24]. A TIA for cardiac EIT applications was designed in 180 nm with a transimpedance gain of 9.5 dBΩ and 6 MHz bandwidth. This TIA consumes 549 µW power from a 3.3 V power supply [25]. The proposed FDLN-TIA exhibits 193.24 dBΩ and a bandwidth of 38.71 MHz. This TIA is implemented in 45 nm CMOS technology. It exhibits ultra-low input referred noise current of 0.95 fA/√Hz and an output-noise voltage of 1.72 pV/√Hz. This FDLN-TIA consumes 8.31 µW from a 1 V power-supply. It exhibits a high CMRR of 88.27 dB, PSRR of 76.35 dB, SNR of 237 dB and a FoM of 4.76×10^{35}. The performance parameters of the modified FDLN-TIA significantly improved in terms of trans-impedance gain, bandwidth, gain-bandwidth product, input referred noise current, output noise voltage, SNR, CMRR, PSRR, FoM and low power consumption.

5 CONCLUSIONS

A CMOS-based modified FDLN-TIA has been implemented in this paper. The proposed FDLN-TIA outperforms in terms of low input-referred-noise-current, low output noise voltage, high trans-impedance gain, wide bandwidth, high Signal-to-Noise Ratio, high Figure of Merrit and low power consumption. The FDLN-TIA exhibits a high trans-impedance gain of 193.24 dBΩ and a wide bandwidth of 38.71 MHz. The input-referred noise-current and the output-noise voltages are minimized by the modified fully differential architecture by using very good layout matching techniques. The proposed FDLN-TIA exhibits a very low input-referred noise-current of 0.95 fA/ √Hz and an output noise voltage of 1.72 pV/√Hz. The FDLN-TIA exhibits a high SNR of 237 dB at 38.71 MHz and the FoM of 4.76×10^{35}. The high CMRR of 88.27 dB and the PSRR of 76.35 dB provide better noise cancellation to achieve low noise. This FDLN-TIA consumes 8.31 µW power at 27 °C from a 1 V supply voltage. All the performance metrics are measured from the post-layout simulations. The proposed FDLN-TIA is implemented in a 45 nm CMOS technology and it occupies a layout area of 61.29 µm × 60.61 µm. From the analysis, it is evident that the FDLN-TIA outperforms well when compared to the other TIAs in the literature. This FDLN-TIA is more suitable for noise-sensitive biosensing applications such as non-invasive blood glucose monitoring that require low noise and low-power consumption.

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6 REFERENCES

[1] Qasemi, S. R., Rafati, M., & Amiri, P. (2019). A 10 Gb/s noise-canceled trans-impedance amplifier for optical communication receivers. *Analog Integrated Circuits and Signal Processing*, *101*(3), 669-680. https://doi.org/10.1007/s10470-019-01546-3

[2] Badal, M. T. I., Reaz, M. B. I., Yeng, L. S., Bhuiyan, M. A. S., & Haque, F. (2019). Advancement of CMOS transimpedance amplifier for optical receiver. *Transactions on Electrical and Electronic Materials*, *20*, 73-84.

https://doi.org/10.1007/s42341-018-00092-5
[3] Li, D., Minoia, G., Repossi, M., Baldi, D., Temporiti, E., Mazzanti, A., & Svelto, F. (2014). A low-noise design technique for high-speed CMOS optical receivers. *IEEE Journal of Solid-State Circuits*, *49*(6), 1437-1447. https://doi.org/10.1109/JSSC.2014.2322868
[4] Sadeghi, S., Nayeri, M., Dolatshahi, M., & Moftakharzadeh, A. (2021). An active CMOS optical receiver employing an inductor-less, low-noise, and high-gain regulated cascode transimpedance amplifier. *Microelectronics Journal*, *110*, 105015. https://doi.org/10.1016/j.mejo.2021.105015
[5] Kira, A., Elsayed, M. Y., Allidina, K., Chodavarapu, V. P., & El-Gamal, M. N. (2021). A 6.89-MHz 143-nW MEMS oscillator based on a 118-dBΩ tunable gain and duty-cycle CMOS TIA. *Electronics*, *10*(21), 2646. https://doi.org/10.3390/electronics10212646
[6] Liu, Y., Gu, K., Liu, X., Li, Y., & Sun, P. (2024). A low noise capacitance to voltage readout circuit based on active feedback charge sensitive amplifier for micro-gyro. *Review of Scientific Instruments*, *95*(6). https://doi.org/10.1063/5.0186178
[7] Royo, G., Sánchez-Azqueta, C., Gimeno, C., Aldea, C., & Celma, S. (2016). Programmable low-power low-noise capacitance to voltage converter for MEMS accelerometers. *Sensors*, *17*(1), 67. https://doi.org/10.3390/s17010067
[8] Ma, R., Liu, M., Zheng, H., & Zhu, Z. (2018). A 77-dB dynamic range low-power variable-gain transimpedance amplifier for linear LADAR. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, *65*, 171-175. https://doi.org/10.1109/TCSII.2017.2684822
[9] Sporrer, B., Wu, L., Bettini, L., Vogt, C., Reber, J., Marjanovic, J., & Huang, Q. (2017). A fully integrated dual-channel on-coil CMOS receiver for array coils in 1.5–10.5 T MRI. *IEEE Transactions on Biomedical Circuits and Systems*, *11*(6), 1245-1255. https://doi.org/10.1109/TBCAS.2017.2764443
[10] Ngo, T. H., Lee, T. W., & Park, H. H. (2011). 4.1 mW 50 dBΩ 10 Gbps transimpedance amplifier for optical receivers in 0.13 μm CMOS. *Microwave and Optical Technology Letters*, *53*(2), 448-451. https://doi.org/10.1002/mop.25741
[11] Cenkeramaddi, L. R., Singh, T., & Ytterdal, T. (2009). Inverter-based 1V transimpedance amplifier in 90nm CMOS for medical ultrasound imaging. *NORCHIP*, 1-4. https://doi.org/10.1109/NORCHP.2009.5397856
[12] van Willigen, D. M., Kang, E., Janjic, J., Noothout, E., Chang, Z. Y., Verweij, M. D., & Pertijs, M. A. (2021). A transceiver ASIC for a single-cable 64-element intravascular ultrasound probe. *IEEE Journal of Solid-State Circuits*, *56*(10), 3157-3166. https://doi.org/10.1109/JSSC.2021.3083217
[13] Tan, M., Chen, C., Chen, Z., Janjic, J., Daeichin, V., Chang, Z. Y., & Pertijs, M. A. (2018). A front-end ASIC with high-voltage transmit switching and receive digitization for 3-D forward-looking intravascular ultrasound imaging. *IEEE Journal of Solid-State Circuits*, *53*(8), 2284-2297. https://doi.org/10.1109/JSSC.2018.2828826
[14] Niranjan, V. & Jhamb, M. (2023). Design of a low-power 180 nm broadband CMOS transimpedance amplifier for biomedical & IoT applications. *International Journal of Information Technology*, *15*(5), 2741-2745. https://doi.org/10.1007/s41870-023-01315-6
[15] Romanova, A. & Barzdenas, V. (2022). On noise modeling of capacitive feedback transimpedance amplifiers in CMOS. Applied Sciences, *12*, 10186. https://doi.org/10.3390/app121910186
[16] Hsu, C. L., Jiang, H., Venkatesh, A. G., & Hall, D. A. (2015). A hybrid semidigital transimpedance amplifier with noise cancellation technique for nanopore-based DNA sequencing. *IEEE Transactions on Biomedical Circuits and Systems*, *9*(5), 652-661. https://doi.org/10.1109/TBCAS.2015.2496232
[17] Yang, T. & Holleman, J. (2015). An ultralow-power low-noise CMOS biopotential amplifier for neural recording. *IEEE Transactions on Circuits and Systems II*: *Express Briefs*, *62*(10). https://doi.org/10.1109/TCSII.2015.2457811
[18] Chaddad, A. (2014). Low-noise front-end receiver dedicated to biomedical devices: NIRS acquisition system. *Circuits and Systems*, 2014. https://doi.org/10.4236/cs.2014.58021
[19] Liang, Y. X. (2023). Low-noise high-gain large-bandwidth transimpedance amplifier with cascode-type preamplifier for cryogenic STM. *Journal of Low Temperature Physics*, *210*, 357-375. https://doi.org/10.1007/s10909-022-02855-0
[20] Romanova, A. & Barzdenas, V. (2019). A review of modern CMOS transimpedance amplifiers for OTDR applications. *Electronics*, *8*, 1073. https://doi.org/10.3390/electronics8101073
[21] Nagulapalli, R., Zourob, S., Hayatleh, K., Yassine, N., Barker, S., & Venkatareddy, A. (2017). A compact high gain opamp for biomedical applications in 45nm CMOS technology. *2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology* (RTEICT), 231-235. https://doi.org/10.1109/RTEICT.2017.8256592
[22] Kim, J., Kim, J., & Ko, H. (2015). Low-power photoplethysmogram acquisition integrated circuit with robust light interference compensation. *Sensors*, *16*(1), 46. https://doi.org/10.3390/s16010046
[23] Puttananjegowda, K. & Thomas, S. (2020). A low-power low-noise multi-stage transimpedance amplifier for amperometric-based blood glucose monitoring systems. *Analog Integrated Circuits and Signal Processing*, *102*, 659-666. https://doi.org/10.1007/s10470-020-01600-5
[24] Wang, W., Zeng, W., & Sonkusale, S. (2021). A low-noise current readout architecture with 160 dB transimpedance gain and 1.3 MHz bandwidth. *Microelectronics Journal*, *108*, 104984. https://doi.org/10.1016/j.mejo.2020.104984
[25] Teng, Y. C. & Odame, K. M. (2022). A CMOS monolithic amplifier for cardiac EIT applications. *Analog Integrated Circuits and Signal Processing*, *112*(3), 443-456. https://doi.org/10.1007/s10470-022-02071-6

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