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# Novel Modular Multilevel Inverter Structures with Reduced Components for Medium Voltage Applications

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**Abstract:** Multilevel inverters (MLIs) are increasingly prominent in medium-voltage and high-power applications due to their ability to produce output voltages with reduced harmonic distortion and lower device blocking voltage. By employing isolated voltage sources, clamping diodes, and flying capacitors, MLIs generate terminal voltages in incremental steps, mimicking a sinusoidal waveform. However, the cascaded structure often requires a higher number of power components as voltage levels increase, resulting in elevated implementation costs. To address these challenges, this article introduces two novel modular MLI structures that utilize fewer semiconductor switches and DC sources to achieve the desired voltage levels efficiently. Each structure employs four DC sources and a reduced number of switches to synthesize stepped voltages at the load terminals, providing a cost-effective and modular solution. The feasibility of the proposed structures is demonstrated through a detailed comparison with recent reduced-component MLI configurations in terms of controllable switches, gate isolators, current-conducting switches, and power loss. The designs are validated using MATLAB/Simulink simulations, and their practicality is confirmed through real-time performance analysis using a laboratory prototype. The results show strong agreement between simulated and experimental findings, confirming the proposed designs' effectiveness.

**Keywords:** harmonic distortion; MATLAB/simulink validation; modular structures; multilevel inverters (MLI); reduced component design

## 1 INTRODUCTION

The Multilevel Inverter (MLI) spawns higher voltage steps in contrast with two level inverters to use in medium voltage higher power applications. It uses small voltage sources like batteries or DC link to formulate output voltage in staircase shape with lower Total Harmonic Distortion (THD). The voltage rating of switching devices used in MLI is lower than the overall output voltage which means that the voltage is shared between the switches due to cascade connection. MLI expands its wide spread applications like reactive power compensator, E-Vehicle (EV), adjustable speed drives and non-conventional Energy Sources [1-3]. The fundamental operating principle of MLI is realized using classical MLIs namely Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge Inverters (CHBMLI) [4]. The first two topologies work well for five level operation; beyond that it requires higher voltage rating switches, clamping diodes and capacitors make inverter complex. This problem can be assuaged by cascading several H-Bridge inverters to form CHBMLI. This topology is free from capacitor unbalancing problems, requirement of higher rating switches and clamping capacitors. However, the use of switching devices increases with increase in voltage levels. Several researches put forth to carve out new MLI structures with different perspectives and some other way by restructuring the traditional topologies in hybrid form [5-8].

Two new variants in MLI topologies for single-phase supply are developed to function in symmetrical and asymmetrical configurations. The topology is suggested for use in electrical drives and the integration of non-conventional energy resources. The structure utilizes two input dc supplies, twelve controlled switches, one clamping capacitor, and three diodes to create boosted thirteen-levels and seventeen-levels for symmetric and asymmetric operation respectively [9]. Two new MLI circuits that use less controllable semiconductor IGBTs have been addressed to overcome boundaries of classical topologies. The first MLI uses lesser count of switches and second MLI avails minimum input dc supplies to cause a high number of voltage steps [10]. A bidirectional asymmetrical multilevel inverter (MLI) has been presented which needs a single input dc supply and lower device constituents. The inverter circuitry comprises an H-bridge on the primary side of the high frequency transformer and asymmetrical modules on the secondary side. The developed topology has the capability of making the ac output voltage with up to fifteen levels [11].

A new MLI ensuing formation is composed of a number of incorporated units and every unit is organized with several cascaded basic units. Each unit has an isolated input dc supply, a bypassing diode and a controllable device. The Proper switching sequence between the dc power supplies in different units envisages high number of voltage steps. A method to balance the input dc power supplies which needs high-frequency magnetic-link to formulate the inverter is also presented [12]. A hybrid cascaded multilevel converter has been presented which is proficient in engendering double the voltage levels as that caused by a classical CHBMLI. The topology comprises a T-type H-bridge power cell and the left over are series combination of identical H-bridge inverters. The power sharing is equal in both H-Bridge and transistor clamped cells [13]. A new twin T-type thirteen level inverter has been presented to offer lesser IGBTs, gate isolators and diodes than fresh MLI. The topology requires no supplementary circuits to balance the capacitor voltage [14].

A modified structure for nine level inverter using a dual dc link and eight switches has been presented with dual dc links arranged in a ratio of 1:3. The topology claims more efficient due to the use of fewer conducting switches and does not need a backend H-bridge [15-18]. A compact cascaded MLI has been developed using series connected sub modules. The mixture of basic cells and polarity reversal circuit forms the SM. Owing to its modular structure, the developed MLI can be comprehended to achieve higher voltage steps. A quadruple boosting nine-level inverter has been developed to offer lesser components using only ten semiconductor switches, three

uncontrolled switches and two capacitors for nine- level operation. The topology requires sensorless operation and the capacitor voltages are self balanced through series-parallel combination. A cascaded half-bridge MLI using switched-capacitors has been developed that requires only one dc source and it requires less switches, unprompted capacitor charging and voltage boosting effects. The developed topology eliminates inter module leakage currents. A topology is constituted by using two MPUC7s in cascaded connection supplied by only one input dc power supply through a high-frequency link (HFL). It produces maximum of 49- steps using four unequal dc links, twelve controllable switches and one HFL unit [19-23].

A nine-level inverter using single-source has been developed that uses minimum power devices and utilizes switched capacitors as virtual dc sources to reduce active dc sources. The switched capacitors have the ability of self-charging with naturally balancing. A multilevel inverter structure requires six IGBTs and one bidirectional IGBT to produce 7- and 11- steps in the output voltage in equal and unequal input power supplies with the inherent feature of generating possible voltage levels [24-27]. A new MLI circuit is made up of three capacitors and eight controllable semiconductor switches to produce seven-level output voltage. Boost operation is possible and the output voltage has boosted 1.5 times of the input voltage. A suitable switching pattern using SPWM is discussed to balance the capacitor voltage. A new single phase asymmetrical MLI has been developed to generate 33- levels with less switches withstanding lower blocking voltage. The circuit can be scaled up by cascading the circuits for higher voltage steps [28-31].

A detailed technical review from the recent literature, more noteworthy MLI structures have been presented in the recent years to reduce power switches and dc sources for higher number of levels, but each topology has its own operating characteristics when dc source values are different. In this research, a new inverter circuitry is conceived to trim down overall switch counts and switches in current conduction path compared with traditional topologies. The working principle and gating sequence generation to emulate the stepped voltage using the developed topology is formulated in this paper. The feasibility of the new MLI is verified using Matlab/Simulink R2018b and a standard experimental setup is arranged to confirm the simulation results.

## 2 PROPOSED METHOD

### 2.1 Operating Principle of Developed Symmetrical and Asymmetrical Module

The purpose of developing MLI topology is to attain good power quality by means of shaping the load voltage closer to sinusoidal and inherit the characteristics to diminish lower order harmonics magnitudes and reduce THD. However, the MLI topologies require switching devices and dc sources to linearly increase with voltage levels. In this work, an attempt has been made to achieve remarkable voltage levels with reduction in IGBTs and input power supplies. The other important attributes of the developed topology is the reduced number of switches in current path which leads to less conduction loss. The anticipated topology uses four dc sources associated with few semiconductor switches to connect/disconnect with the load and an H-bridge inverter to form a modular structure. Two level synthesizing structures have been developed to achieve stepped voltage at the H-Bridge inverter input terminals for MLI. The first structure uses the same value of voltage sources which is also called symmetrical structure to produce 9- level voltage. The second module uses different values of input voltage sources to elevate from symmetrical structure as asymmetrical module with two more switches added to operate the voltage sources ($V_2$, $V_3$ and $V_4$) independently to attain voltage levels higher than symmetrical MLI. Fig. 1 portrays the developed level synthesizing modules which are composed of four voltage sources ($V_{1E}$, $V_{2E}$, $V_{3E}$ and $V_{4E}$) and controlled switches ($S_{1E}$-$S_{9E}$) respectively. There are six operating sequences for symmetrical module with the same value of voltage sources to result in 9- level inverter as shown in Figs. 2 and 3 respectively. In Mode-1, the switches ($S_{1E}$ and $S_{7E}$) are switched into conduction state to add the voltage source ($V_{1E}$) to the load. The switches ($S_{2E}$ and $S_{7E}$) are turned into ON state to add the input voltage supplies ($V_{1E}$ + $V_{2E}$) to the load in Mode- 2. The voltage sources ($V_{1E}$ + $V_{2E}$ + $V_{3E}$) are connected to the load by switching the switches ($S_{2E}$ and $S_{5E}$) in Mode- 3. The load is connected to the voltage sources ($V_{1E}$ + $V_{2E}$ + $V_{3E}$ + $V_{4E}$) through the switches ($S_{2E}$ and $S_{4E}$) in Mode- 4. The switches ($S_{3E}$ and $S_{6E}$) are turned into conduction to obtain Mode- 5 and Mode- 6 respectively.

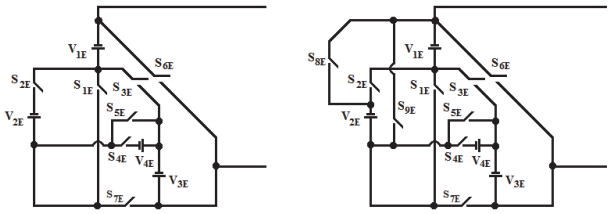


**Figure 1** Developed level synthesizing modules (a) Symmetrical (b) Asymmetrical

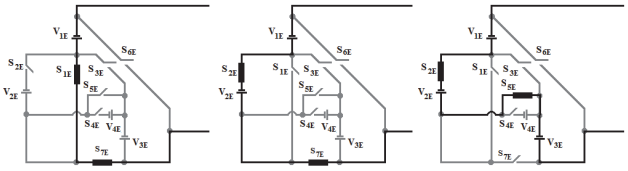

**Figure 2** Operating sequences for symmetrical module (a) Mode-1 (b) Mode-2 (c) Mode-3

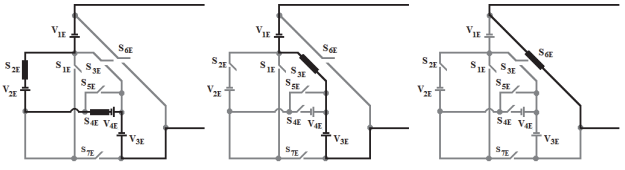

**Figure 3** Operating sequences for symmetrical module (a) Mode-4 (b) Mode-5 (c) Mode-6

The blocking voltage across IGBTs in the proposed symmetrical module is given in Eqs. (1)-(6) as:

$$VS_{1E} = V_{1E} \tag{1}$$

$$VS_{2E} = VS_{7E} = V_{1E} + V_{2E} \tag{2}$$

$$VS_{3E} = V_{1E} + V_{3E} \quad (3)$$

$$VS_{4E} = V_{3E} + V_{4E} \quad (4)$$

$$VS_{5E} = V_{4E} \quad (5)$$

$$VS_{6E} = V_{1E} + V_{2E} + V_{3E} + V_{4E} + V_{5E} \quad (6)$$

Two switches ($S_{8E}$ and $S_{9E}$) are added to symmetrical module to obtain the operation of connecting the voltage sources ($V_{1E}$, $V_{2E}$ and $V_{3E}$) independently to the load. This arrangement makes the possibility of having different values of source voltages to elevate the voltage levels.

Fig. 3 shows the operating sequence to connect the voltage sources ($V_{1E}$, $V_{2E}$ and $V_{3E}$) independently with different voltage values to acquire higher voltage steps. In mode-1, the switches ($S_{7E}$ and $S_{8E}$) are switched to connect the voltage $V_{2E}$ to the load. Similarly, the switches ($S_{5E}$, $S_{9E}$) and ($S_{4E}$, $S_{9E}$) are made to conduct to connect the input voltage supplies ($V_{3E}$ and $V_{4E}$) to the load. The addition of these two switches ($S_{8E}$, $S_{9E}$) in symmetrical module makes flexibility in arranging different voltage source magnitudes by means of source magnitude computation methods. Tabs. 1 and 2 tabulate the methodology to determine the source values with different combinations. The symmetrical and asymmetrical modules facilitate to generate higher voltage steps with lesser switches using the methods portrayed in Tabs. 1 and 2 respectively.

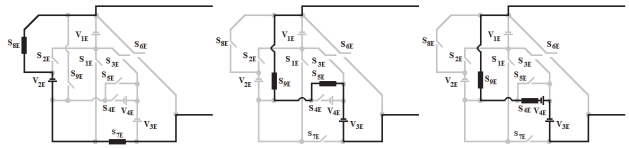

**Figure 4** Operating sequences for Asymmetrical module (a) Mode-1 (b) Mode-2 (c) Mode-3

**Table 1** Methods to evaluate the values of voltage sources in the new symmetrical topology

| Method | Magnitude of voltage sources | Peak output voltage / $V_{max}$ | Voltage levels / m | Operation |
|---|---|---|---|---|
| **1** | $V_{1E} = V_{2E} = V_{3E} = V_{4E} = V_{dc}$ | $V_{max} = (4 \times E \times V_{dc})$ | $V_{max} = (8 \times E) + 1$ | Symmetrical |
| **2** | $V_{1E} = V_{2E} = (2^{E-1})V_{dc}$<br>$V_{3E} = V_{4E} = (2^{E})V_{dc}$ | $V_{max} = 6\sum_{j=1}^{E} 2^{j-1} V_{dc}$ | $12\sum_{j=1}^{E}\left(2^{j-1}\right)+1$ | Asymmetrical |
| **3** | $V_{1E} = V_{2E} = (4^{E-1})V_{dc}$;<br>$V_{3E} = V_{4E} = (2\times(4^{E-1})V_{dc})$ | $V_{max} = 6\sum_{j=1}^{E} 4^{j-1} V_{dc}$ | $12\sum_{j=1}^{E}\left(4^{j-1}\right)+1$ | Asymmetrical |

**Table 2** Methods to evaluate the values of voltage sources in the new asymmetrical topology

| Method | Magnitude of voltage sources | Peak output voltage / $V_{max}$ | Voltage levels / m | Operation |
|---|---|---|---|---|
| 1 | $V_{1E} = V_{2E} = V_{3E} = V_{4E} = (4E-1)V_{dc}$ | $V_{max} = 4\sum_{j=1}^{E} 4^{j-1} V_{dc}$ | $8\sum_{j=1}^{E}\left(4^{j-1}\right)+1$ | Asymmetrical |
| 2 | $V_{1E} = (4E-1)V_{dc}$;<br>$V_{2E} = V_{3E} = V_{4E} = (2\times(4E-1)V_{dc})$ | $V_{max} = 7\sum_{j=1}^{E} 4^{j-1} V_{dc}$ | $14\sum_{j=1}^{E}\left(4^{j-1}\right)+1$ | Asymmetrical |
| 3 | $V_{1E} = (8E-1)V_{dc}$;<br>$V_{2E} = V_{3E} = V_{4E} = (2\times(8E-1)V_{dc})$ | $V_{max} = 7\sum_{j=1}^{E} 8^{j-1} V_{dc}$ | $14\sum_{j=1}^{E}\left(8^{j-1}\right)+1$ | Asymmetrical |

From the Tab. 1, it is seen that there are three methods to compute the magnitude of voltage sources to achieve greater value of voltage levels. The developed MLI uses two symmetrical modules with 8 dc sources and 18 switches, the Method-I performs symmetrical operation which produces 17- level, the other two are asymmetrical operation: Method-II results in 37- level and method-III generates 61- level respectively. The maximum number of switches in current conduction path is 6. Out of 6 switches, four switches are PWM modulated with blocking voltage and two switches are fundamental switching with high blocking voltage. Similarly in Tab. 2, for the same two modules, the asymmetrical module requires 22 switches and 8 dc sources; the Methods (I, II and III) generate 41, 71 and 127 voltage levels. The addition of two switches in symmetrical modules results in marginal increase in total switch count; however, the number of voltage levels (Method-III) is higher compared with symmetrical modules for the same number of dc power supplies. It is seen that the proposed MLI generates more voltage levels with reduced switches in overall power component count and in the current conduction path to attain lesser power loss with better efficiency. The methods formulated for both modules for asymmetrical operations show different voltage levels for various input voltage values as shown in Figs. 4 and 5 respectively.

### 2.2 Comparison Study between Developed and Recent Reduced Count MLI Topologies

The other important parameter for realizing the feasibility of the proposed symmetric and asymmetric modules is by means of comparing typical parameters like IGBTs, gate drivers, current conducting switches and power loss. The developed symmetrical module is compared with recent reduced count MLIs in terms of the above parameters besides different voltage levels. Figs. 6, 7 and 8 portray the comparison chart for requirement of IGBTs, gate isolators and switches in current path for various combinations of voltage levels. It is seen from the plots that the developed symmetrical module requires least components compared with recent reduced count topologies. This implication shows that the proposed symmetrical module with an H-Bridge inverter is well suited for cascaded operation to achieve different voltage levels in higher order for various combinations of voltage determination algorithms. Similarly, the developed asymmetrical module requires only two switches more than the proposed symmetrical module which leads a marginal increase in the total power components and results in great increase in voltage steps using the Method-3 tabulated in Tab. 2.

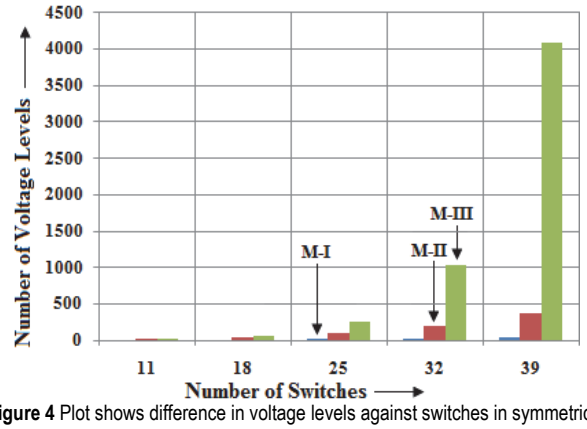


**Figure 4** Plot shows difference in voltage levels against switches in symmetrical module

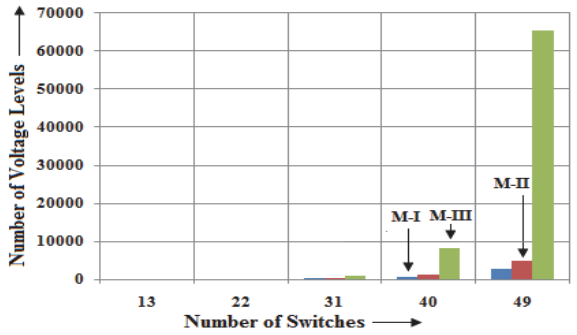


**Figure 5** Plot shows difference in voltage levels against switches in asymmetrical module

It is important to explore the merits of the proposed symmetric and asymmetric modules in terms of total cost. The cost function is an important factor to distinguish the proposed level generation modules (symmetric/asymmetric) from recent reduced count asymmetrical topologies. The cost factor depends on Total Standing Voltage (*TSV*), Peak Inverse Voltage (*PIV*), Maximum output voltage ($V_{max}$) and number of switches ($N_{sw}$). The cost function can be expressed in Eq. (7) as:

$$Cost\ Function\ (CF) = N_{sw} + \left[(\chi * TSV)/V_{max}\right] + \left[(\sigma * PIV)/V_{max}\right] \quad (7)$$

$\chi$ is the weight factor of *TSV* against $N_{sw}$ and $\sigma$ is the weight factor of PIV against $N_{sw}$. The values for $\chi$ and $\sigma$ are selected in such a way that their value is greater than 1 while the *TSV* and *PIV* are more important than Nsw. Similarly, ($N_{sw}$) is considered more important, the $\chi$ and $\sigma$ is lesser than 1. Tab. 3 tabulates the values of *CF* for proposed and recent reduced count topologies for different $\chi$ and $\sigma$. It is seen from the Tab. 6 that the cost function calculated for higher voltage levels is lower compared to the recent reduced count topologies listed in the same table and its value increases as it gets into lower number of values levels. It is evident that the proposed MLI holds better position in *CF* also.

**Table 3** Comparison between proposed modules and recent reduced count asymmetric topologies in terms of TSV, PIV and CF for different voltage levels

| Reduced count MLIs | Classification | Voltage ratio | No. of voltage levels | Total standing voltage | *PIV* | Cost Factor per level (*CF*) | |
|---|---|---|---|---|---|---|---|
| | | | | | | $\chi = \sigma = 0.5$ | $\chi = \sigma = 1.5$ |
| [44] | Asymmetrical | 1:2:4:8 | 31 | 90Vdc | 12Vdc | 0.496774 | 0.716129 |
| [45] | Asymmetrical | 1:2:7:14 | 49 | 96Vdc | 21Vdc | 0.294643 | 0.394133 |
| [46] | Asymmetrical | 3*n*–1 | 17 | 36Vdc | 6Vdc | 0.742647 | 1.051471 |
| [47] | Asymmetrical | 2*n*–1 | 15 | 28Vdc | 4Vdc | 0.952381 | 1.257143 |
| [48] | Asymmetrical | 1:2 | 23 | 12Vdc | 10Vdc | 1 | 1.086957 |
| [49] | Asymmetrical | 1:3 | 15 | 28Vdc | 6Vdc | 0.828571 | 1.152381 |
| [50] | Asymmetrical | 1:3:7:15 | 31 | 50Vdc | 15Vdc | 0.392473 | 0.532258 |
| [51] | Asymmetrical | 1:2*n* | 15 | 42Vdc | 15Vdc | 0.738095 | 1.280952 |
| [52] | Asymmetrical | 1:2 | 11 | 23Vdc | 5Vdc | 0.981818 | 1.490909 |
| Symmetrical module (A3) | Asymmetrical | (1:2)4*n*–1 | 61 | 80Vdc | 24Vdc | 0.323497 | 0.380328 |
| Asymmetrical module (A3) | Asymmetrical | (1:2)8*n*–1 | 127 | 200Vdc | 48Vdc | 0.188726 | 0.219723 |

## 2.3 Power loss study

The developed MLI uses less number of IGBTs for *m* level and requires only two switches to conduct current per module in its entire mode of operation. This shows a noteworthy improvement over recent reduced count topologies in asymmetrical modes of operation. The power loss in controllable switches in the developed topology can be broadly classified in two parts: conduction and switching losses [43]. Conduction loss is calculated by the switches and diode in conduction path (8)-(9) and is defined as

$$P_{Cond.Loss}(t) = P_{Loss.switch}(t) + P_{Loss.Diode}(t) \quad (8)$$

$$P_{Cond.Loss}(t) = \left(\left[V_T + R_T I^{\beta}{}_m(t)\right] + \left[V_D + R_D I_m(t)\right]\right) I_m(t) \quad (9)$$

where $V_T$ and $V_D$ are the threshold voltage to make into conduction of the semiconductor switches and diodes, $R_T$ and $R_D$ are the on state of diode resistance and series resistance of capacitor in controlled switch and Im is the peak value of the output current and $\beta$ is a constant. The conduction loss is deliberated by adding the loss earned by the switches during conduction in each level. In the developed MLI, the IGBTs in the conduction path are limited to two for each module, while the traditional CHBMLI and recent reduced count topologies varied with voltage level. For a case study, the developed topology is formulated to function in asymmetrical mode using one module. It produces 15- level with four switches (two from the proposed module and two from H-Bridge) in conduction path and for the same level, the CHBMLI requires eight switches. Therefore, the conduction loss occurred in the proposed topology is halved as that of CHBMLI.

Similarly, the switching loss for a switch during conduction and non-conduction is given by

$$P_{\text{switching.loss},E} = \int_{o}^{t} V(t)i(t)\,\mathrm{d}t = \frac{V_{\text{stand},E} I(t_{\text{on}} + t_{\text{off}})f_s}{6} \quad (10)$$

where, $V_{\text{stand}}$, $E$, $I$ and $f_s$ are the total blocking voltage of the semiconductor switches, current carried by the switches and switching frequency respectively. Let us assume that the on-time and off- time are equal, then the Eq. (10) becomes

$$P_{\text{switching.loss},E} = \frac{V_{\text{stand},E} I(t_{\text{on}})f_s}{3} \quad (11)$$

$$P_{\text{switching.loss},E} = C \times f_s \times V_{\text{stand},E} \quad (12)$$

It is seen in Figs. 2 and 3 that the switches ($S_{6E}$ and $S_{7E}$) have the chance of switching at fundamental frequency and the switch ($S_{3E}$) has another option of connecting the voltage sources ($V_{1E}$ and $V_{3E}$) to the load. In the developed symmetrical module, $V_{11} = V_{21} = V_{31} = V_{41} = V_{51} = V_{\text{dc}}$ to obtain 9- level in the output voltage, the total blocking voltage across the PWM operated switches is calculated as $V$stand, $E = 6\ V_{\text{dc}}$, then the switching loss is derived as (13)

$$P_{\text{switching.loss},E} = 6 \times C \times f_s \times V_{\text{dc}} \quad (13)$$

For the same 9- level CHBMLI, the total standing voltage across the switch is determined as

$$P_{\text{switching.loss,CHBMLI}} = 16 \times C \times f_s \times V_{\text{dc}} \quad (14)$$

It is concluded that the switching loss occurred in the developed topology is lesser than CHBMLI and the conduction loss is half the value of CHBMLI.

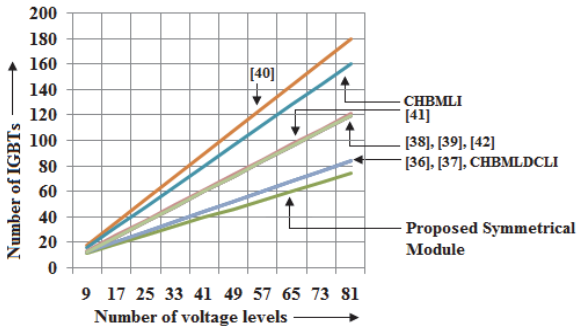


**Figure 6** Comparison Plot between IGBT switches and voltage steps

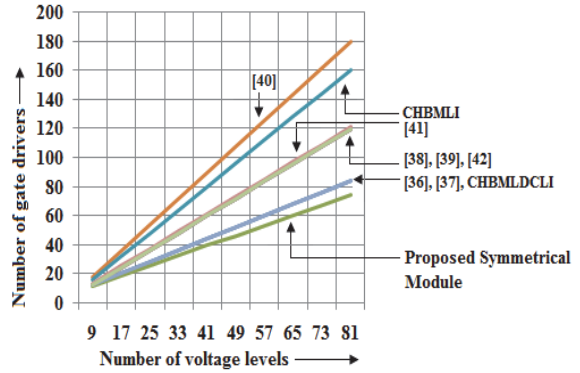


**Figure 7** Comparison Plot between gate drivers and voltage steps

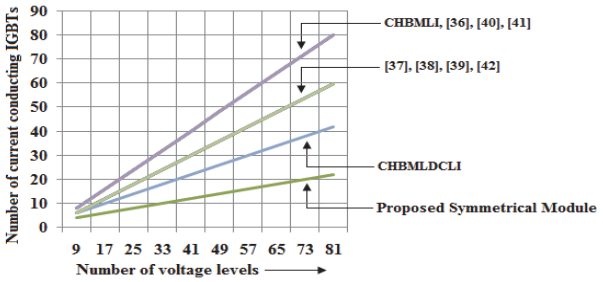


**Figure 8** Comparison Plot between current conducting switches and voltage steps

## 3 SIMULATION RESULTS

The Simulink model for the developed symmetrical and asymmetrical modules is constructed in Matlab R2018b software. The symmetrical module with input voltage source voltages ($V_{1E} = V_{2E} = V_{3E} = V_{4E} = 75$ V) is considered to produce 9- level output voltage to feed RL load values of ($R = 100\ \Omega$ and $L = 100$ mH) respectively. Similarly, for asymmetrical module, the input voltage source values are taken as ($V_{1E} = 40$ V; $V_{2E} = V_{3E} = V_{4E} = 80$ V) to generate 15- level output voltage for the same RL load. The gating pulses are generated using Level Shifted Phase Disposition PWM (LS-PDPWM) with carrier frequency of 2 kHz and fundamental switching at 50 Hz respectively. The symmetrical and asymmetrical modules require 4 and 7 carrier signals to propel PWM pulses for 9- and 15- level inverters. MCPWM is used to produce PWM signals for the IGBTs used in the suggested topology. The scheme propels synthesizing base PWM signals for each level by comparing high frequency triangle carrier and reference sine signals. The base PWM for each level is generated using XOR logical function between present and succeeding level PWM pulses. For instance for level 1 PWM generation, logical XOR-ing the PWM for level 1 and 2 to get level- 1 pulses is as shown in Fig. 9.

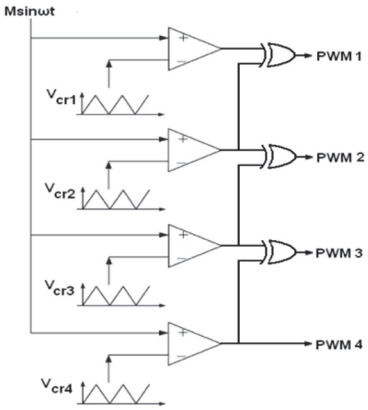


**Figure 9** Simplified Modulation scheme for single phase nine level inverter

The switching sequence for each level has been obtained using the scheme and the VHDL coding is used to generate the desired PWM pulses suitably to generate each level in the output voltage. The Figs. 10 and 11 portray the output voltage and inductive load current waveform for 9- level inverter. The harmonic spectrum for output voltage is shown in Fig. 12 which gives the fundamental voltage of 212 V (rms) and THD of 13.48%. Similarly, the output voltage and inductive load current for 15- level inverter using proposed asymmetrical module is

pictured in Figs. 13 and 14 respectively. The harmonic spectrum for output voltage for 15- level inverter is also shown in Fig. 15 which shows the fundamental voltage of 196.5 V (rms) and THD value of 8.62% respectively. It is clear from the Figs. 12 and 15 that the quality of output voltage is improved with reduced harmonic distortion due to increase in voltage steps in the output voltage from 7 to 15- level inverters.

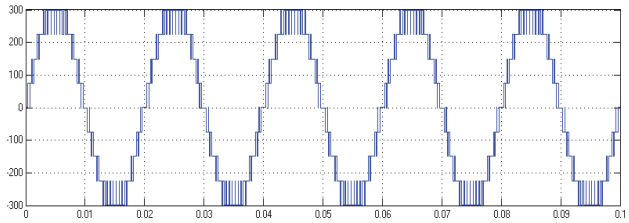

**Figure 10** Output voltage for 9- level inverter

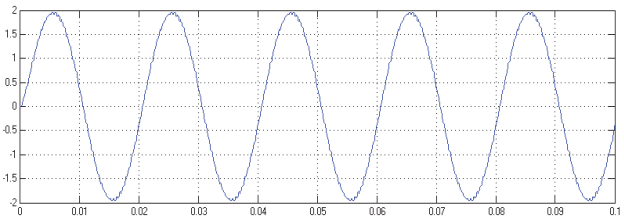

**Figure 11** Inductive load current for 9- level inverter

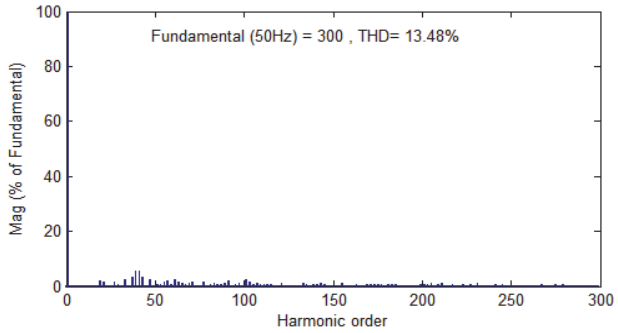


Fig. **Figure 12** Harmonic spectrum for 9- level output voltage

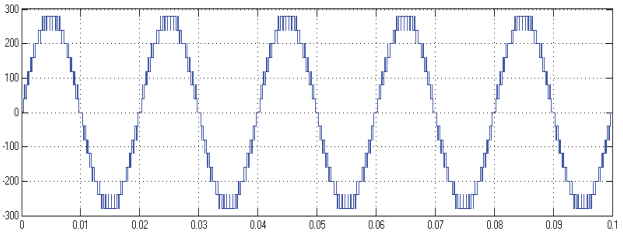

**Figure 13** Output voltage for 15- level inverter

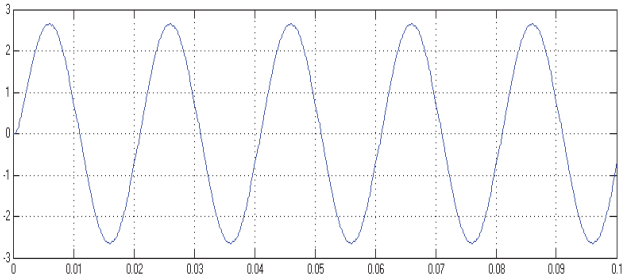

**Figure 14** Inductive load current for 15- level inverter

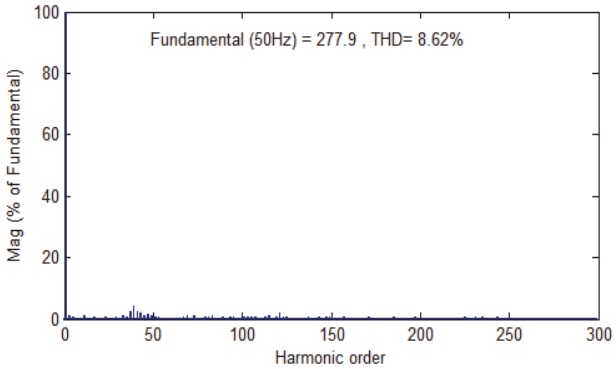


**Figure 15** Harmonic spectrum for 15- level output voltage

## 4 EXPERIMENTAL RESULTS

The developed symmetrical and asymmetrical modules used in simulation study are constructed in laboratory prototype. The experimental setup consists of several isolated IGBT modules along with associated gate driver circuits and these modules are tailored based on design requirement. The switches IGBT (SGW20N60) with a power rating of (600 V/20 A) and bi-directional IGBT (FIO 50-12BD) with a rating of 1200 V/50 A are used to construct the isolated switch module. The input dc supply is obtained through diode bridge (KBPC2504- 400 V/25 A) and a dc-link capacitor of 5000 uF to smoothen input dc voltage and the same value of RL load is used in experimental arrangement. The experimental gating signals are generated using Xilinx Spartan 3E-500 FG320 FPGA controller. The methods follow reference sine data as LUTs and separate up/down counters are used to generate triangle carrier for each level. The developed topology uses fundamental switching which can be obtained by using two counters to generate 50 Hz square pulses.

**Table 4** Comparison of simulation and experimental results

| Sl. No | Simulation | | Experimental | |
|---|---|---|---|---|
| | Fundamental output voltage | THD / % | Fundamental output voltage | THD / % |
| 9- Level inverter | 212.1 | 13.48 | 201.7 | 13.5 |
| 15- Level inverter | 196.5 | 8.62 | 196.1 | 8.69 |

## 5 CONCLUSION

A new MLI for symmetrical and asymmetrical topologies using two novel level generation modules has been formulated in this paper. The novel level generation modules use fewer switches/dc sources which are modular and utilize only two switches in current conduction path in each module. The developed MLI topologies proclaim their advantages in terms of usage of lesser IGBTs, isolated input dc power supplies, number of output voltage levels, gate driver units, total power losses over traditional and recently developed topologies. Due to its modularity, the developed MLI is well opted for medium voltage high power applications. Three new methods are derived to elucidate the values of input voltage sources to generate different varieties of voltage levels using developed modules. The simulation and experimental results for 9-level and 15-level inverters have been demonstrated to

authenticate the feasibility of the developed MLI for renewable energy interfaces.

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