INFLUENCE OF CARRIER DISTRIBUTION ON THE HALL MOBILITY OF THIN SILICON-ON-SAPHIRE (SOS) FILMS

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Typical results of the gated-Hall-bar measurements on SOS films[1] (Fig.1) show the significant variation of the Hall mobility with gate voltage V_G. Surface scattering can not explain the behaviour in Fig.1 completely.

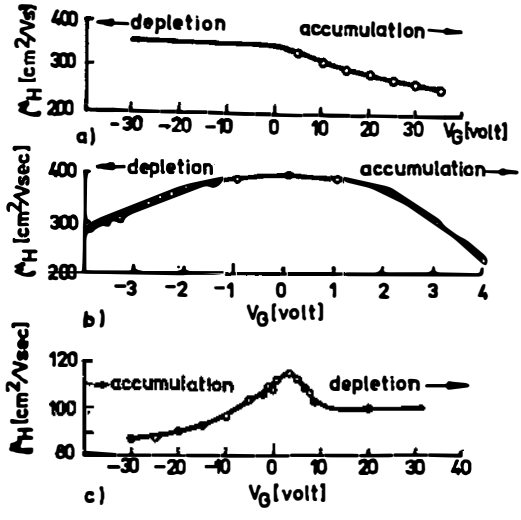

Fig.1. Hall mobility μ_H versus gate voltage V_G for silicon-on sapphire films[1]

a) Low resistivity n-type.
b) Medium resistivity n-type.
c) Medium resistivity p-type.

Experimentally verified dependence of hole an electron mobilities[2] μ_p and μ_n of the distance from the Si-SiO_2 inter-face can explain some region of μ_H-V_G curve[1]. For example, if gate voltage accumulates carriers in the high-mobility region, the averaged μ_H increases. To verify Fig. 1 analytically, we start from the well-known Petritz[3] expression for average Hall mobility:

$$\mu_H = \frac{\int_0^d p(z)\mu_p^2(z)dz - \int_0^d n(z)\mu_n^2(z)dz}{\int_0^d \mu_p(z)p(z)dz + \int_0^d \mu_n(z)n(z)dz} \qquad (1)$$

where p(z) and n(z) are hole and electron concentration, d- the Si film thickness, and z- the distance from Si-surface.

The experimental results[2] give us $\mu_p(z)$ and $\mu_n(z)$. With the known surface potentials ψ_1 (at Si-SiO_2 interface) and ψ_2 (at Si- sapphire interface) we can obtain n(z) and p(z) dependences[4]. So, the main problem is to determine ψ_1-V_G and ψ_2-V_G dependences. Our method earlier developed for sandwich MISIM structure[4] can be used with two modification: 1.- We include fast surface states. Thus, surface charge becomes gate-voltage dependent, 2.- Due to the not parallel equipotential planes, we must use another boundary condition at Si-sapphire interface. It is shown[5] that in all real cases we can neglect leakage electric field lines in sapphire. So, this boundary condition becomes $E_2 = Q_{S2}/\varepsilon_S$, where E_2 and Q_{S2} are electric field and surface charge at Si-sapphire interface and ε_S is the dielectric constant.

With these modifications, we can construct two equation for ψ_1 and ψ_2. Numerical calculations show that not only ψ_1 but also ψ_2 are very sensitive to the gate voltage shanges. This means that Si surface 1 - surface 2 interaction is significant. For some gate voltage in Si film can exist not only full depletion but also full accumulation. Both results are consequences of a finite thickness of semiconducting films.

Preliminary numerical calculations applied to (1) give a qualitative agreement. For the quantitative agreement we must be certain of the preciseness in some experimental data used.

References

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