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Original scientific paper

In-depth Analysis of the Control Unit for Multiple Voltage Rails to Drive a Variety of ICs

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Abstract: Generating a negative output voltage rail from a positive input voltage is possible by reconfiguring an ordinary buck regulator into an inverting buck-boost (IBB) topology. Rather than operating considerations such as voltage and current stresses, the main challenge associated with this transformation arises from differences in the small-signal closed-loop characteristics. The most critical distinction is the presence of a right-half-plane (RHP) zero in the control-to-output transfer function of the IBB, which introduces non-minimum-phase behaviour, reduces the achievable phase margin, and may lead to instability and poor load transient response. For conventional PI controllers, the buck and IBB converters resulted in settling times of 5.0 ms and 6.8 ms, with overshoots of 13.65% and 8.46%, respectively, thus demonstrating the performance limitations of fixed-gain designs. As a solution, an auto-tuned PI controller with adaptive features has been proposed, which operates effectively in both the buck and IBB topologies. The proposed scheme achieves a significantly faster settling time of 2.27 ms with overshoot and undershoot below 2%, thereby ensuring superior robustness and dynamic performance compared to conventional approaches.

Keywords: adaptive control; auto-tuned PI controller; inverting buck-boost topology; negative voltage generation; sensitivity analysis

1 INTRODUCTION

A wide range of electrical and power system applications, including operational amplifier circuits, analogue signal processing, and systems requiring bipolar power supplies, depend on negative voltage generation [1-3]. It is essential for providing a steady reference voltage for precise measurement and control, or for powering particular components that need a negative supply to function properly [4, 5]. Even yet, it can be difficult to achieve negative voltage effectively and economically, especially when considering variables like power efficiency, control complexity, and flexibility [6, 7].

Linear regulators, charge pump circuits, and specialised DC-DC converters are examples of conventional techniques for producing negative voltage [8]. Although linear regulators are straightforward, they are inefficient, particularly when high power levels are needed [9]. Because charge pump circuits rely on capacitor switching, they may not be appropriate for high power applications or systems that need precise voltage regulation, despite their efficiency [10, 11]. DC-DC converters, like the inverting buck-boost converter, on the other hand, provide a more effective and adaptable solution [12, 13]. Nevertheless, these converters frequently call for unique layouts and extra control circuitry, which can raise the complexity and expense [14].

Generating negative voltage by transforming a standard DC-DC buck converter into a buck-boost converter using the same control unit is a novel method developed to eliminate the problems in the above-mentioned techniques and their applications [15]. In the reconfiguration process, all it takes to accomplish the transition is to change the DC input voltage and grounding which reduces the need for extra hardware. Although utilizing the existing control scheme is one of the most important advantages of this proposed method in terms of system simplicity and efficiency, it poses a problem of inability to run properly for multiple operating points of varying dynamic models [16-18]. Compared with the minimum-phase buck converter, boost-derived topologies such as the inverting buck-boost (IBB) operate in continuous-conduction mode (CCM) with a right-half-plane zero (RHPZ) in the control-to-output path, which makes feedback design substantially more delicate [19, 20]. Physically, a duty-ratio increase initially diverts energy into the inductor (shorter diode/secondary conduction interval), so the output voltage moves in the opposite direction before recovering, an inverse response that is the hallmark of non-minimum-phase (NMP) behavior [21]. In CCM this is captured by the RHP zero of the control-to-output transfer function, whose location depends on the operating point. The immediate consequence is a hard upper bound on achievable closed-loop bandwidth and phase margin; good practice is to limit the crossover to a fraction of this zero [22]. Moreover, operating-point changes that increase duty cycle or decrease load shift RHPZ toward the origin, tightening the bandwidth constraint and making the loop more fragile. These properties explain why controller synthesis for IBB/boost converters is more challenging than for buck converters [23].

Considering the mathematical models of the buck converter and the buck-boost converter obtained after reconfiguration, the requirement of a sophisticated control technique is evident. In this context, multi-objective control techniques emerge as a relevant consideration and many studies on this topic have been conducted recently in a wide range of fields [24-30].

This study presents an in-depth analysis highlighting the necessity of an adaptive, single integrated control unit by examining the step-response characteristics of both topologies. The transfer functions of the buck and IBB converters were derived, and fixed-gain PI controllers were designed accordingly. Although applying these controllers separately improves the open-loop response of the systems, their performance was found to be insufficient across varying operating conditions. To address this limitation, an auto-tuned PI controller with adaptive features was developed, effectively overcoming the shortcomings of conventional fixed-gain designs.

2 POWER STAGE DESIGN EQUATIONS

The buck converter used in this study was developed specifically to take in an input voltage (V_{in}) of 50 volts and

transform it into an output voltage (V_{out}) of 25 volts. The switching frequency (f_{sw}) at which the converter operates is 10 kHz. The minimum load resistance (R_{min}) under maximum load conditions has been determined to be 5 ohms. The maximum ripple allowed for the inductor during CCM operation is 20% of the average inductor current (I_L) and the maximum load. Likewise, a maximum ripple of ±2% of the average output voltage (V_C) is permitted for the capacitor.

The parameters and design equations of the buck converter discussed in the study are given in Tab. 1.

2.1 Open-Loop Block Diagram Outputs

MATLAB/Simulink® software is used to model the suggested buck converter using computed values and ignoring parasitic resistances. The MOSFET's diode resistance (R_d) and internal resistance (R_{on}), both expressed in ohms (Ω), are set at 0.001. Similarly, the default value of 0.001 is used for the diode internal resistance $R_{d(on)}$, expressed in ohms (Ω). Furthermore, a load step of 2 A is applied to the output resistance instead of a steady load to observe the transient response of the system.

Table 1 Parameters and design equations of the proposed buck converter

Parameter	Steady-state Duty Cycle	Average Inductor Current	Inductor Ripple Current	Boundary Condition Current	Boundary Condition Load	Inductance	Average Output Voltage	Capacitor Ripple Voltage	Capacitance
Symbol	D	I_L	ΔI_L	$I_{L(B)}$	R_B	L	V_C	ΔV_C	C
Equation	$\frac{V_{out}}{V_{in}}$	$\frac{V_{out}}{R_{min}}$	$0.2 \times I_L$	$\frac{\Delta I_L}{2}$	$\frac{V_{out}}{I_{L(B)}}$	$\frac{V_{in}(1-D)D}{f_{sw}\Delta I_L}$	V_{out}	$0.04 \times V_{out}$	$\frac{V_{in}(1-D)D}{8Lf_{sw}^2\Delta V_C}$
Value	0.5	5	1	0.5	50	1.3	25	1	12.5
Unit	-	A	A	A	Ω	mH	V	V	µF

The converter operates with an input voltage (V_{in}) of 50 V, an output voltage (V_{out}) of 25 V, a switching frequency (f_{sw}) of 10 kHz, and a minimum load resistance (R_{min}) of 5 Ω.

Fig. 1 shows the output voltage and inductor current waveforms of the proposed buck converter in presence of a step change of the load at 4 ms.

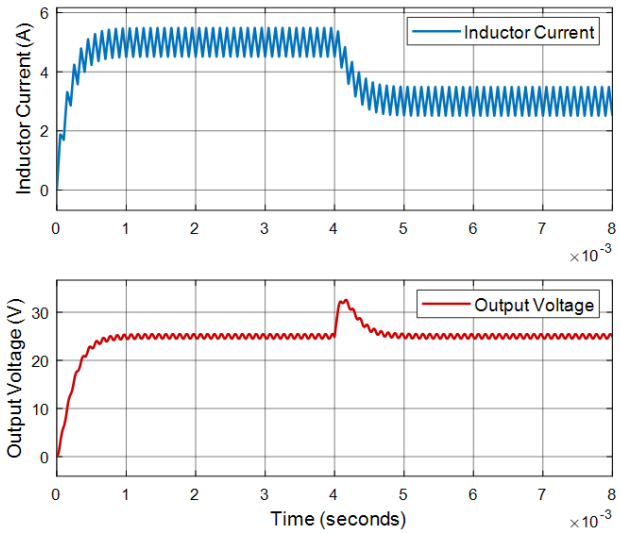

Figure 1 Output voltage and inductor current waveforms in the presence of a step change

Signal statistics such as maximum, minimum, peak-to-peak, mean, median, and root mean sqaure (RMS) are vital for analyzing a signal's behavior. Maximum and minimum define amplitude limits, while peak-to-peak shows the dynamic range. Mean and median indicate central tendency, with median being less sensitive to outliers. RMS is key for assessing effective power. Together, these metrics offer a clear view of signal quality and stability in the time domain.

It has been observed that the buck topology's voltage and current waveforms exhibit the anticipated outcomes in accordance with the computed values. Tab. 2 provides the signal statistics of the waveforms acquired in Fig. 1.

Table 2 Signal statistics of the voltage and current waveforms

Signal Statistics	Inductor Current / A	Output Voltage / V
Maximum	5.486	32.58
Minimum	0	0
Peak-to-peak	5.486	32.58
Mean	3.938	24.17
Median	3.771	25.03
RMS	4.1	24.6

Fig. 2 shows the output voltage waveforms of the buck-boost converter that was restructured from the intended buck topology in the presence of the load step change at 4 ms, as well as the total voltage across the controller and the switches.

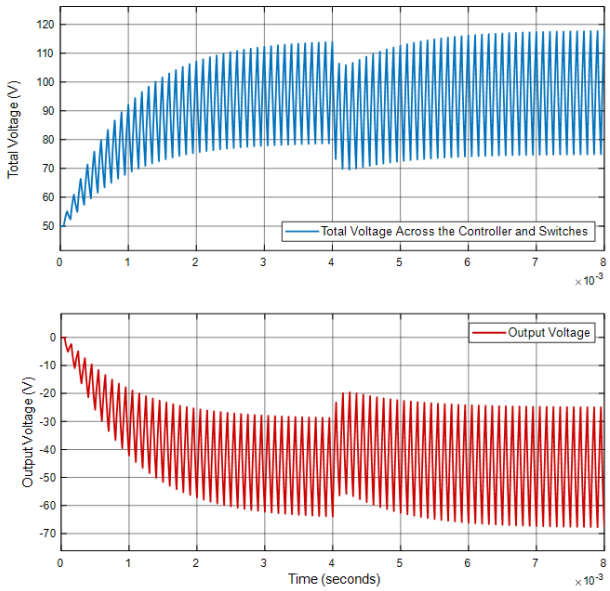

Figure 2 Total and output voltage waveforms of the IBB

It has been observed that the voltage waveforms in the new configuration exhibit significantly large ripples, which may affect the overall performance and reliability of the system. This irregular behavior suggests inadequate filtering or improper control response. To support this observation, detailed signal statistics corresponding to the waveforms presented in Fig. 2 are summarized in Tab. 3.

Table 3 Output and total voltage waveforms signal statistics of the IBB

Signal Statistics	Inductor Current / A	Output Voltage / V
Maximum	19.54	0
Minimum	0	−72.41
Peak-to-peak	19.54	72.41
Mean	15.08	−41.29
Median	16.05	−41.59
RMS	15.59	44.43

It should be noted that a direct transition between the buck and the IBB topologies cannot be achieved under open-loop control due to the significant differences in their small-signal characteristics. To evaluate the feasibility of operating with a single fixed controller originally designed for the buck converter, the effects of switching frequency and load variations were deliberately examined. These controlled changes provide insight into how the reconfigured system behaves under different operating conditions, thereby highlighting the robustness of the proposed control strategy rather than indicating arbitrary parameter adjustments.

Fig. 3 shows how output voltage ripples are impacted by different switching frequencies for the buck-boost configuration.

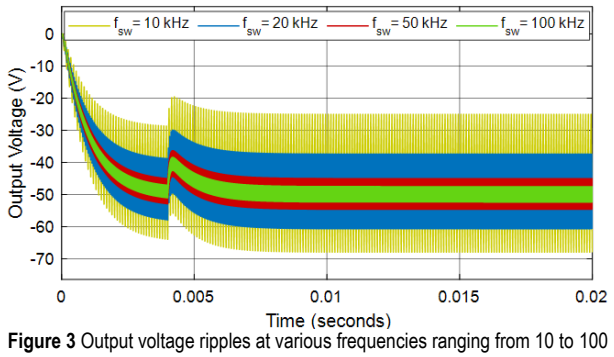

Figure 3 Output voltage ripples at various frequencies ranging from 10 to 100 kHz

The effect of various resistive output loads on output voltage ripples is illustrated in Fig. 4.

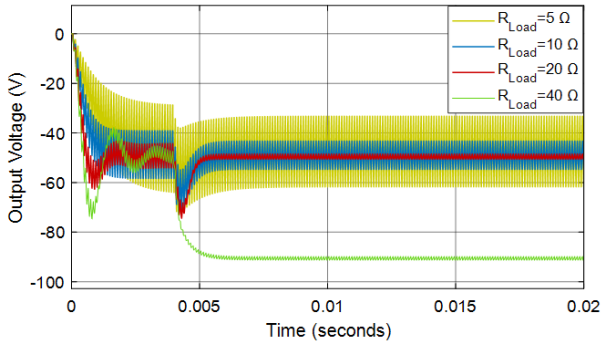

Figure 4 Output voltage ripples at various loads ranging from 5 to 40 Ω

The intention of this work is not to redesign a new controller for each operating point, but to emphasize that a single, fixed design, originally developed for the buck converter, can still operate effectively under different conditions after reconfiguration. Therefore, the variations in switching frequency and load represent controlled operating scenarios that highlight the robustness and adaptability of the proposed scheme, rather than uncontrolled parameter changes. This approach underlines the novelty of the study: instead of developing separate designs for buck and IBB converters, the same hardware and control structure can be employed seamlessly in both topologies.

3 COMPUTER AIDED TRANSFER FUNCTION ESTIMATION

Simulink® Control Design™ is employed to derive the transfer functions of both buck and buck-boost (reconfigured from buck topology) converters. The procedure of estimating the transfer function involves gathering frequency response data from the Simulink model of the proposed converters, whose specifications are listed in Tab. 1. The values assigned for the switching circuit elements (Insulated-gate Bipolar Transistor (IGBT) and Diode) used in the analysis are included in Tab. 4 and 5 for a more realistic analysis rather than being chosen as ideal.

Table 4 IGBT characteristics employed in the designed power stage

Parameter	Value	Unit
Forward Voltage	0.1	V
On-state Resistance	1×10^{-6}	Ω
Off-state Conductance	1×10^{-6}	1/Ω
Threshold Voltage	0.5	V
Integral Diode Forward Voltage	0.1	V
Integral Diode On-state Resistance	1×10^{-6}	Ω
Integral Diode Off-state Conductance	1×10^{-6}	Ω

Table 5 Diode characteristics employed in the designed power stage

Parameter	Value	Unit
Forward Voltage	0.8	V
On-state Resistance	1×10^{-6}	Ω
Off-state Conductance	1×10^{-6}	1/Ω
Zener Resistance	0.3	Ω
Reverse Breakdown Voltage	inf	V
Junction Capacitance	0	pF

3.1 Transfer Function Estimation of the Proposed Buck Converter

A buck converter's transfer function can be described utilising the relationships between its various interacting factors. The study of interest in this paper is the transfer function from the PWM duty cycle set-point to the load voltage. By adding disturbance to the duty cycle set-point via sinusoids with different frequencies and storing the load voltage appropriately, frequency response data is gathered.

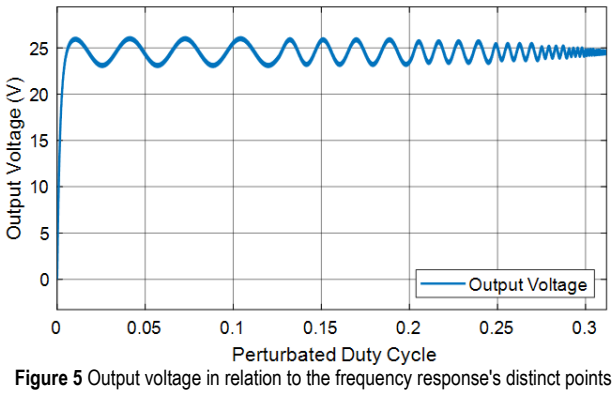

Figure 5 Output voltage in relation to the frequency response's distinct points

The frequency range of the carried-out signal is between 200 and 20000 rad/s of the switching frequency.

This implementation's primary goal is to ascertain how the system alters the injected sinusoidal signals' phase and magnitude. In other words, the output is the load voltage, and the frequency input point is the duty cycle. The operational duty cycle in the steady state of 0.5 is perturbed by 0.03 sinusoids injected at the input point. Output voltage with respect to the discrete points on the frequency response is given in Fig. 5.

Bode Frequency response of the proposed system is given in Fig. 6.

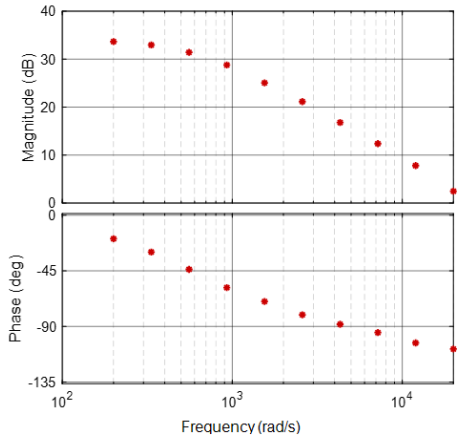

Figure 6 Bode plot of the system

The Bode response reveals a system that matches what is expected for this circuit with a high frequency roll-off of about 20 dB/decade, no resonance, and a 35 dB gain. Data on frequency response is gathered in the preceding stage. The fitted transfer function (duty cycle to buck converter output voltage) to the data is provided as follows in Eq. (1), and this data depicts the system as discrete frequency points:

$$\frac{V_{\text{Buck(out)}}}{D} = \frac{3464s + 1.281\times10^{9}}{s^{2} + 4.312\times10^{4}s + 2.518\times10^{7}} \tag{1}$$

To confirm the accuracy of the estimated transfer function, its response and the discrete points are plotted in Fig. 7.

The model of the derived transfer function of the proposed buck converter is estimated with a 99.09% value of match, a final prediction error of 0.0685 and a mean square error of 0.0294.

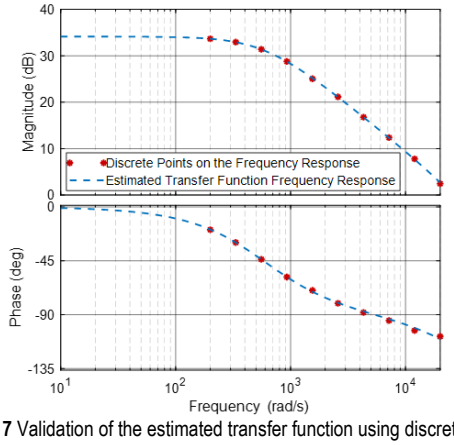

Figure 7 Validation of the estimated transfer function using discrete frequency response points

3.2 Transfer Function Estimation of the Restructured Buck (Buck-Boost) Converter

Considering the effect of the switching frequencies in Fig. 3 and the resistive loads in Fig. 4 on the output voltage ripples, in the new configuration, the switching frequency is determined as 20 kHz instead of 10 kHz and the resistive output load is determined as 40 ohms instead of 5 ohms. In addition, since the voltage on the control unit and switching elements is produced not only by the input voltage source but also by the circuit itself, a capacitor with a value of 1 μF has been added here. The reconfiguration from buck to the IBB topology is realized simply by relocating the power supply and grounding, i.e., connecting the negative terminal of the output capacitor to the supply ground. This modification changes the reference polarity of the output voltage and leads to the observed 180° phase inversion in the frequency response. The consistency between the analytical transfer functions and discrete simulation points verifies the validity of the model, while future work will focus on experimental confirmation.

Fig. 8 displays the output voltage with respect to the discrete points on the frequency response for the reconfigured buck converter topology.

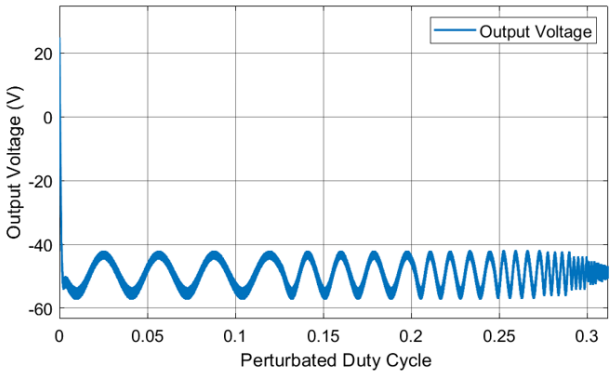

Figure 8 Output voltage plotted against discrete frequency response points for the reconfigured buck converter topology

Fig. 9 shows the restructured system's Bode Frequency response. It illustrates the gain and phase behavior across a range of frequencies, providing insight into the system's stability and dynamic characteristics. Key features such as bandwidth, resonance, and phase margin can be observed from the plot.

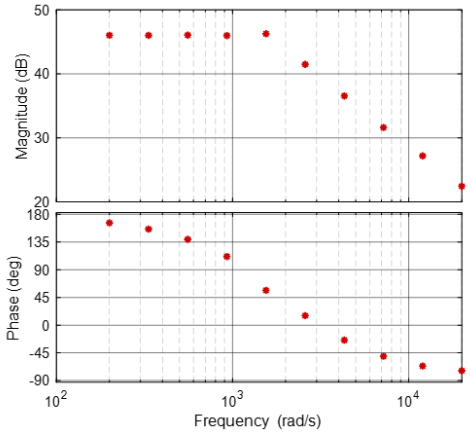

Figure 9 Bode frequency response illustrating the dynamic behaviour of the restructured system

The buck-boost topology's Bode response reveals a system with a gain of approximately 48 dB, relatively mild resonance around 1800 rad/s, and a high frequency roll-off of about 20 dB/decade. The data presents the buck-boost topology as discrete frequency points, and the fitted transfer function (duty cycle to buck-boost converter output voltage) to the data is given as follows:

$$\frac{V_{\text{Buck-boost(out)}}}{D} = \frac{2.545\times10^{5}s - 5.55\times10^{8}}{s^{2} + 2278s + 2.826\times10^{6}} \tag{2}$$

The response of the estimated transfer function and the discrete points are plotted in Fig. 10 to verify its accuracy.

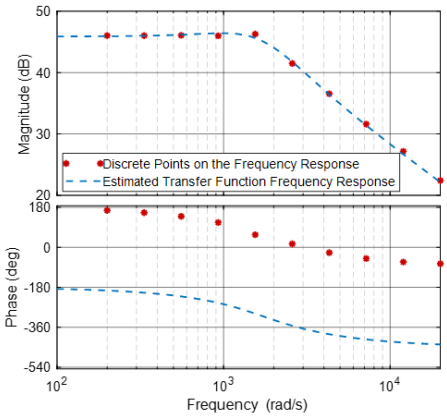

Figure 10 Comparison of restructured buck converter's estimated transfer function with discrete frequency response points

The estimated model of the derived transfer function of the proposed buck converter has a mean square error of 105.7, a final prediction error of 246.6, and a match percentage of 92.42%. The discrete points and the resultant transfer function curve diverge by 180 degrees (180° phase shift), as can be seen when examining the phase graph in Fig. 10. This situation is due to negative voltage production and looking at the numerator part of the transfer function in Eq. (2), right half plane zero confirms this. When the signs of the s term and the constant term in the numerator are changed, it will be observed that the 180° phase difference will disappear. Step responses of the estimated transfer functions are given in Fig. 11.

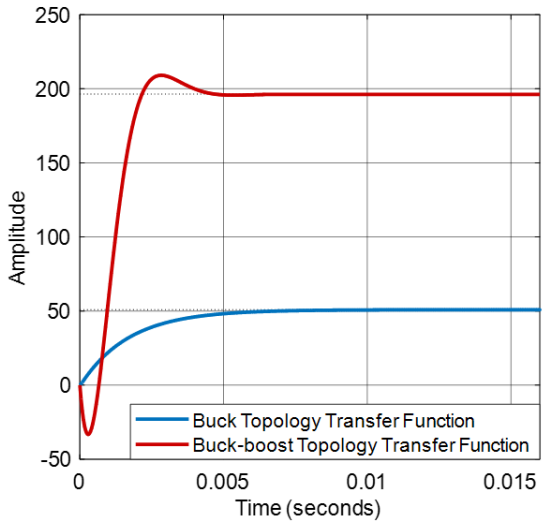

Figure 11 Open-loop step responses of the estimated transfer functions

Tab. 6 presents a comparison of the estimated transfer functions' open-loop step response characteristics.

Table 6 Open-loop step response characteristics of the estimated transfer functions

Open-loop Step Response Characteristics	Estimated Transfer Functions	
	Buck Topology	Buck-boost Topology
Rise Time / s	0.0037	0.0011
Settling Time / s	0.0066	0.0039
Settling Minimum Value	45.9546	209.1049
Settling Maximum Value	50.8724	177.4248
Overshoot / %	0	6.4740
Undershoot / %	0	16.9635
Peak Value	50.8724	209.1049
Peak Time / s	0.0178	0.0028

In the new topology obtained by relocating the input voltage source and grounding, overshoot and undershoot occur compared to the buck converter. This is an important issue that should be taken into consideration during the controller design process, and since the common control unit is aimed in the proposed application, it must work effectively for both situations.

4 VERSATILE PI CONTROLLER DESIGN FOR MULTI-OBJECTIVE CONTROL TASKS

By utilising Simulink® Control Design™ to predict the plant's response and observe its behaviours in both time and frequency domains, the mathematical model of the plant is appropriately obtained. To enhance the plant's important dynamic properties, stability, response time, steady-state error, and oscillations that comprise the transient and steady-state, control systems, the proportional integral (PI) feedback compensator is designed and implemented in this manner. The main motivation for adopting this controller is that the PI feedback compensator structure is a widely used controller due to its attributes of being easy to grasp, simple to create, and simply understood. The generic unity feedback structure of the proposed system is illustrated in Fig. 12. An Auto-tuned PI technique is intended to create the control unit dual purpose because there are mathematical models with distinct characteristics, and a single integrated controls design is the objective.

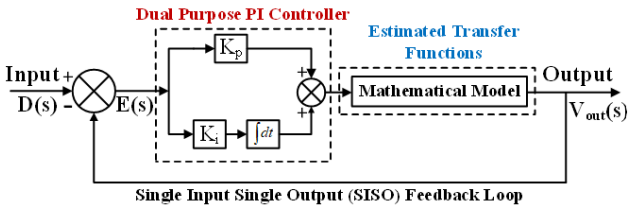

Figure 12 Generic unity feedback control structure of the proposed system

Using the loop-shaping method, the PI controller transfer function of the proposed buck converter is generated as follows:

$$G_{\text{PI(buck)}} = \frac{0.0214s + 36.3}{s} \tag{3}$$

In a similar manner, the PI controller's transfer function for the reconfigured buck converter by

considering the previously mentioned 180° phase shift is produced as follows:

$$G_{\mathrm{PI(buck\text{-}boost)}} = \frac{0.00127s + 2.88}{s} \tag{4}$$

Closed-loop step responses of the estimated transfer functions are given in Fig. 13.

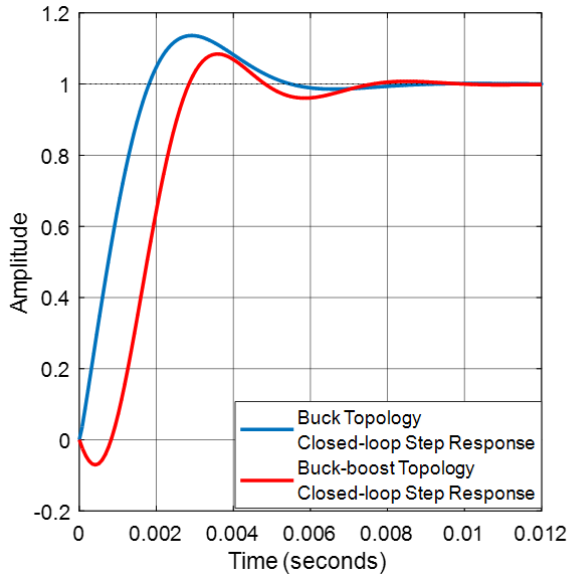

Figure 13 Closed-loop step responses of the estimated transfer functions

Closed-loop step response characteristics of the estimated transfer functions in continuous time are provided in Tab. 7.

Table 7 Closed-loop step response characteristics of the estimated transfer functions

Closed-loop Step Response Characteristics	Estimated Transfer Functions	
	Buck Topology	Buck-boost Topology
Rise Time / s	0.0013	0.0015
Settling Time / s	0.0050	0.0068
Settling Minimum Value	0.9223	0.9286
Settling Maximum Value	1.1365	1.0846
Overshoot / %	13.6484	8.4606
Undershoot / %	0	7.0678
Peak Value	1.1365	1.0846
Peak Time / s	0.0029	0.0036

Fig. 14 shows the general arrangement of a PI autotuner block in a control system in the schematic diagram.

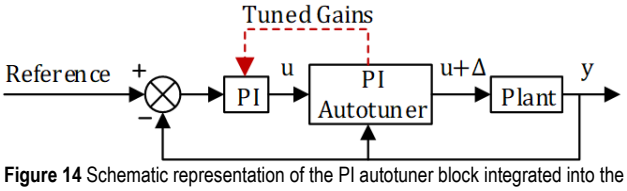

Figure 14 Schematic representation of the PI autotuner block integrated into the control system

Frequency-response estimate and subsequently adjusting the controller gains are the foundations of the auto-tuned PI controller technique, which has rendered the system adaptive. Tuning goal is based on targeted bandwidth and phase margin parameters which are determined by the stability criteria of switch mode power supply given in Tab. 8.

Table 8 Tuning parameters derived from switch-mode power supply stability requirements

Parameters	Value
Crossover (cutoff) frequency	Between the range of $1/10^{th}$ to $1/8^{th}$ of switching frequency
Phase Margin	Greater than 45 degree
Gain Margin	Greater than 10 dB
The slope of the gain curve at the crossover frequency	≈ -20 dB/decade

The auto-tuned PI controller operates based on recursive RMS method and regression. Tab. 9 provides the tuning process workflow.

Table 9 Workflow of the auto-tuning process for the PI controller using recursive RMS and regression methods

Step	Description
Integration	Incorporation of the tuner into the control system to use real-time feedback to adaptively adjust PI gains
Controller Parameters Set-up	Specifying targeted bandwidth and phase margin
Specifying Estimation Parameters	Specifying targeted bandwidth and phase margin
Executing the Tuning Process	Estimation of frequency-response data
Applying Computed Tuned Gains	Application of the tuned proportional and integral gains

A state-level tolerance of 2% is used to analyse the system's settling time, using 90% as the upper reference level and 10% as the lower reference level (rise time from 10% to 90%). These metrics are employed to assess the time-based response characteristics, providing information on the stability and dynamic performance of the system following a step input.

To demonstrate the enhancement achieved with the recommended auto-tuned PI control, the closed-loop system step response together with the results obtained by applying fixed-gain PI controllers derived in Eq. (3) and Eq. (4) separately are given in Fig. 15.

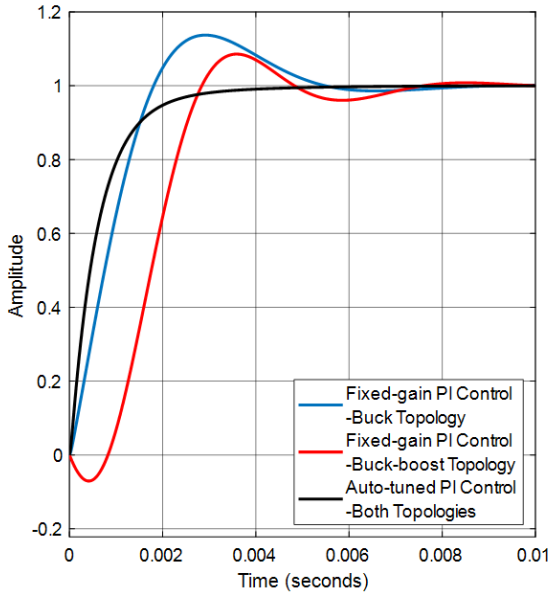

Figure 15 Closed-loop step response comparison between the auto-tuned and fixed-gain PI controllers

The application of the proposed control scheme resulted in an overshoot of 0.310%, an undershoot of 1.998%, and a settling time of 2.268 ms. In comparison to the fixed-gain PI controllers for buck and buck-boost topologies, the proposed controller demonstrates superior performance in terms of reduced overshoot, minimized undershoot, and faster settling time.

5 CONTROL PERFORMANCE ASSESSMENT AND ANALYSIS

Control performance assessment and monitoring are essential in ensuring the efficiency and effectiveness of control systems. These processes involve evaluating how well control systems maintain desired outputs despite disturbances, variations in input and output, parameter uncertainties and transport delay. In this context, the performance of the proposed control scheme is examined in detail by considering all these issues. Analysis is carried out in two stages which are autotuning and implementation of various disturbance. Autotuning process starts at 0.04 seconds and lasts 0.02 seconds since the bandwidth is split by the length of seconds required for the online frequency response calculation to converge, which is approximately 200.

5.1 Input Voltage Variation (±20%)

The effect of ±20 percent variation in input voltage on the system is shown in Fig. 16. The input voltage was changed in steps of 40 V to 50 V at 0.065 s, 50 V to 60 V at 0.07 s, and 60 V to 50 V at 0.08 s. As a results of these step changes, the system exhibited maximum and minimum voltage levels of 26.413 V (refers to 5.65% overshoot), 26.203 V (refers to 4.812% overshoot), and 24.048 V (refers to 3.808% undershoot), respectively. In all three cases, the transient response time was observed to be approximately 600 µs.

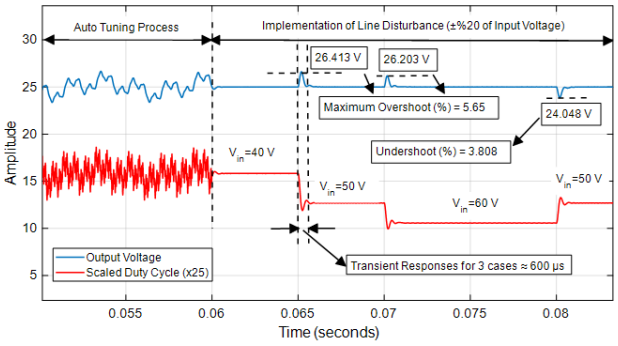

Figure 16 System performance under ±20% variation in input voltage

5.2 Load Current Disturbance (±20%)

The effect of ±20 percent variation in load on the system is shown in Fig. 17. The load was changed in steps of 4 Ω to 5 Ω at 0.065 s, 5 Ω to 6 Ω at 0.07 s, and 6 Ω to 5 Ω at 0.08 s. As a results of these step changes, the system exhibited maximum and minimum voltage levels of 28.54 V (refers to 14.16% overshoot), 27.56 V (refers to 10.24% overshoot), and 22.764 V (refers to 8.944% undershoot), respectively. In all three cases, the transient response time was observed to be approximately 750 µs.

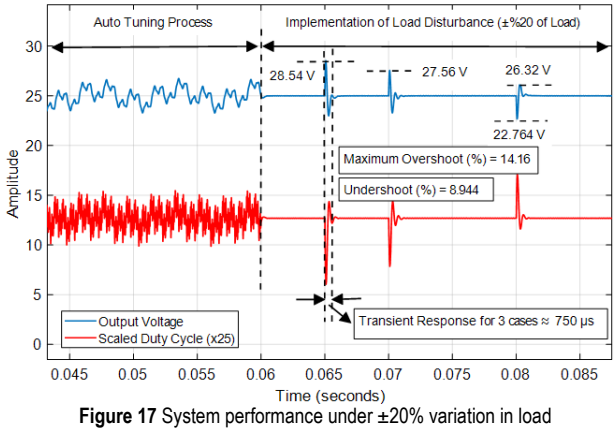

Figure 17 System performance under ±20% variation in load

As highlighted in Tab. 2., the controller parameters were tuned to ensure a phase margin greater than 45° and a gain margin above 10 dB, with the crossover slope adjusted to approximately –20 dB/decade. These margins guarantee closed-loop stability while providing a balance between fast transient response and robustness. Under ±20% load variations, the system exhibited overshoot levels up to 14.16% and undershoot of 8.94%, with a settling time of approximately 750 µs. Such deviations are consistent with the expected behaviour of converters with moderate-to-high phase margins (≈ 54-60°), where limited overshoot is observed but no sustained ringing occurs. In contrast, converters with low phase margins (< 30-35°) typically exhibit much larger overshoot (> 20-25%), pronounced ringing, and longer settling times [31]. For comparison, conventional PI controllers reported in the literature for buck and boost converters usually produce overshoot in the 10-20% range with slower settling times (2-6 ms), whereas the proposed adaptive PI scheme ensures significantly faster recovery and minimal oscillatory behaviour. These findings verify that the adopted design rules not only satisfy the required stability criteria but also provide superior dynamic performance compared to well-established baseline methods [32].

5.3 Parametric Sensitivity Analysis of Passive Circuit Elements

In sensitivity analysis, the design space of the model was created with parameters inductance (L), capacitance (C) and minimum load resistance ($R_{\min}$). For the sensitivity analysis, each parameter is sampled 50 times using a random sampling method. A normal distribution is applied to all parameters to ensure values remain centred around the nominal values. The mean and standard deviation for each parameter are as follows: the C has a mean value of 1.25×10^{-5} and a standard deviation of 7.2169×10^{-7}, the L has a mean value of 0.0013 and a standard deviation of 7.5056×10^{-5}, and the $R_{\min}$ has a mean value of 5 with a standard deviation of 0.2887.

It is aimed to analyse the impact of these parameters on the output voltage and rise time of the system. Maximum value of the output voltage and the rise time (the time the response takes to rise from 10% to 90% of the way from the initial value to the steady-state value) of this signal was assigned as evaluation requirements. The results are demonstrated in Fig. 18.

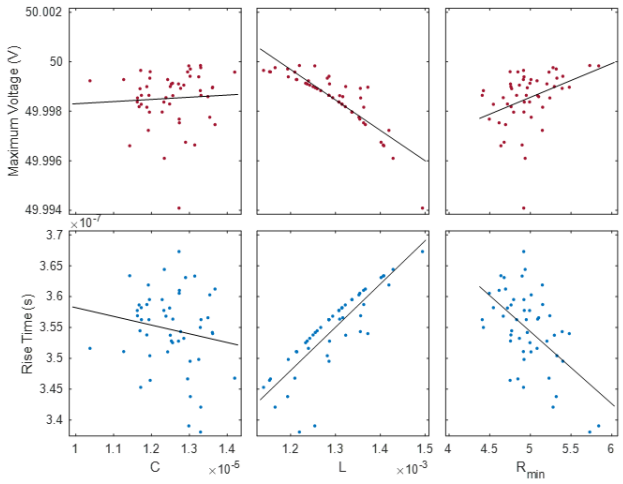

Figure 18 Analysis results showing the effect of parameters on output voltage and rise time using defined performance criteria

The results indicate a clear trend for the *L*, whereas no distinct pattern is observed for the *C* and R_{min} parameters. When comparing *C* and R_{min}, the data points for R_{min} exhibit a slightly higher concentration around a specific region, suggesting a more noticeable clustering effect. An increase in the *L* reduces the maximum output voltage while extending the rise time.

The R_{min} exhibits the opposite effect; however, an analysis of the trend line slope reveals that its impact on rise time is more pronounced compared to its effect on the maximum output voltage. A similar trend is observed for the *C*. However, an analysis of the trend line slopes indicates that *C* does not have a significant impact on both the maximum output voltage and rise time. Given that the slope for rise time is slightly steeper, it can be concluded that the influence of *C* on rise time is more dominant.

Maximum output voltage value is directly proportional to R_{min} and inversely proportional to *L* with a higher impact on the magnitude. On the other hand, the parameter *C* does not significantly affect the output voltage maximum value. In terms of rise time, the *C* value appears to be slightly more effective and is inversely proportional to the requirement, while the situation is the opposite for R_{min} and *L*.

6 CONCLUSION

This study presented an effective method for generating a negative output voltage by reconfiguring a conventional buck converter into an IBB topology. While this transformation introduces control challenges, particularly due to the RHP zero degrading phase margin, an adaptive, auto-tuned PI controller was proposed to address these issues. Unlike conventional PI controllers, which achieved settling times of 5.0 ms (buck) and 6.8 ms (IBB) with overshoots of 13.6484% and 8.4606%, respectively, the proposed controller significantly improved performance, reducing the overshoot to 0.310%, undershoot to 1.998%, and settling time to 2.268 ms.

In addition to steady-state performance, the controller demonstrated exceptional robustness under dynamic conditions. For ±20% load variations, the system responded with a maximum overshoot of 14.16%, a minimum voltage dip of 8.944% undershoot, and consistently achieved recovery within approximately 750 µs. Similarly, during ±20% input voltage disturbances, the system-maintained stability with overshoots below 5.65%, undershoot of 3.808%, and a rapid transient response time of approximately 600 µs. It is worth noting that the impact of the RHPZ is more pronounced under load disturbances than under input voltage variations. This is because load steps directly excite the duty-to-output control path, where the RHPZ inherently limits the achievable transient response, leading to larger overshoot and undershoot. In contrast, input voltage variations affect the system primarily through the line-to-output dynamics, where the influence of the RHPZ is less dominant. This explains why the system exhibited higher deviations under load steps (up to 14.16%) compared to input voltage variations (≤ 5.65%), despite maintaining rapid settling in both cases.

While the proposed auto-tuned PI controller provides robustness and improved transient response, certain limitations should be acknowledged. Future work will therefore include experimental verification and extension of the method to more complex converter architecture.

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