

Compact and High-Performance QCA-Based Adder Design Using an Optimized XOR Logic Structure

V. BHUVANESWARI*, S. YUVARAJ

Abstract: Quantum-dot Cellular Automata (QCA) has emerged as a viable nanotechnology for implementing ultra-dense, low-power digital logic circuits, offering significant advantages over traditional CMOS technology in terms of power consumption and device scalability. This paper presents an efficient design approach for constructing QCA-based half adder and full adder circuits using a novel, highly compact XOR gate configuration. The proposed XOR gate requires only 8 quantum dots, which significantly reduces the overall complexity and area of the arithmetic circuits. The design methodology utilizes the concept of half-cell distance optimization and effective cell-to-cell interaction to achieve reduced latency and minimal crossover usage. The QCADesigner simulation tool is employed to validate the correctness and performance of the proposed circuits. Comparative analysis is carried out against previously reported QCA-based adder designs, considering key performance metrics such as cell count, number of wire-crossings, and propagation delay. The simulation results reveal that the proposed half adder and full adder designs outperform existing counterparts in terms of compactness and operational efficiency. Furthermore, the proposed layouts are fully planar and do not require multilayer crossovers, thereby simplifying fabrication and enhancing practical applicability. The findings demonstrate that the compact XOR gate-based approach provides a scalable and power-efficient solution for implementing fundamental arithmetic operations in future nanoelectronic systems. This work highlights the potential of QCA as a next-generation design paradigm for low-power computing architectures.

Keywords: digital adders; low-power logic design; nano arithmetic circuits; quantum-dot cellular automata (QCA); XOR gate optimization

1 INTRODUCTION

For several decades, the primary option in the field of digital circuit designs has been Complementary Metal-Oxide-Semiconductor (CMOS) technology. Benefits of CMOS include strong noise immunity, scalability, and compatibility with contemporary fabrication techniques [1]. However, CMOS encounters major obstacles such as leakage current, space overhead, and power consumption as technology shrinks in size. Due to these limitations, researchers have found substitute technologies that can overcome them and open up new avenues for computing at the nano-scale.

QCA has evolved as a viable alternative technology for digital circuits in recent years [2]. QCA makes it possible to create low power, high-density digital circuits and presents a viable way around CMOS technology's drawbacks. QCA performs digital computations at the nanoscale level by utilizing the inter-action between the concept quantum dots and physics. Compared to CMOS, this method offers the edge of higher integration densities and better performance metrics.

The adder, which carries out arithmetic operations, is a crucial part of digital circuits. The design of adder elements can maximize the performance of all digital circuits. Addition activities need the use of half adders and full adders [3]. Low area adder circuits are in high demand in contemporary computer applications. However, the adder circuits take up a significant amount of computing resources and complicate low-power applications.

Low-area half adders and full adders are required in a number of applications, such as Internet of Things (IoT) devices, portable electronics, and new technologies. To conserve resources and enable smooth blending into small form factors, these applications frequently require energy-efficient and compact electronics. So designing and creating a new adder circuit is crucial [4].

The design of half adders (HA) and full adders (FA) utilizing QCA technology is the main emphasis of this work. Furthermore, suggested is a brand-new XOR gate

design that uses just eight dots and is dependent on half distance and cell interaction. The overall half adder and full adder design is made more compact and efficient by the usage of this XOR gate [5].

The paper is systematized as follows: The Quantum dots cellular automata preliminary stages were covered in section 2. Related works are compiled under Section 3. A detailed presentation of the suggested XOR, HA, and FA designs is provided in the section 4. Both the results and discussions are shown in section 5. The article is finally brought to a close in section 6.

2 PRELIMINARIES

2.1 QCA

QCA is a computing paradigm based on nano-technology that uses the concepts of quantum mechanics to make a digital computation. QCA depends on the behaviour of quantum dots, which act as binary information carriers. These quantum dots interact with each other, forming logic gates and circuits at the nanoscale level.

2.2 Majority Gate in QCA

The majority gate is the primary component used in QCA circuit design.

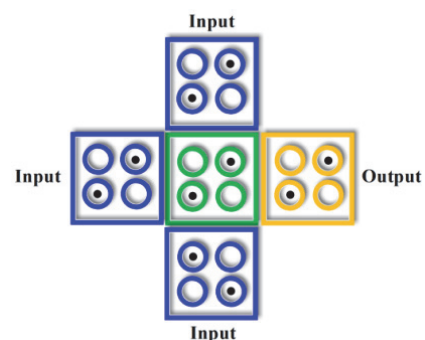


Figure 1 QCA majority gate

It uses a Boolean function to determine which of its inputs is the majority value. The majority gate in QCA is achieved by taking advantage of the Coulombic interaction between adjacent quantum dots. The majority of the gate can be accomplished effectively and consistently by carefully positioning the dots with their polarizations. An essential part of creating intricate QCA circuits is the majority gate. Fig. 1 depicts the majority gate's structure.

2.3 QCA Wire

In QCA, wires are used to propagate and transmit information between different components of a circuit. Unlike conventional electrical wires, QCA wires consist of quantum dots aligned in a straight line. These dots interact with each other, permitting the transmission of binary information. QCA wires must maintain signal integrity and minimize signal distortion to ensure accurate computation within the circuit. Fig. 2 depicts the QCA wire's construction.

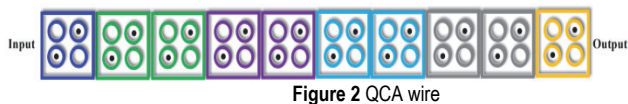


Figure 2 QCA wire

2.4 QCA Inverter

The QCA inverter contains series of quantum dots placed in a specific pattern. These dots interact with each other through the Coulombic forces, allowing for the manipulation of their polarization states. The layout diagram of QCA inverter is shown in Fig. 3.

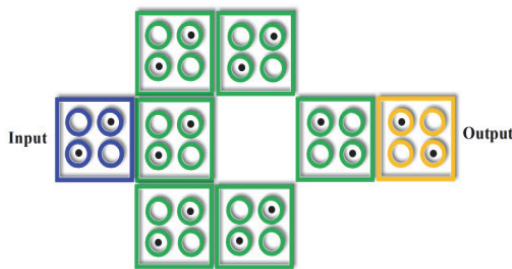


Figure 3 QCA inverter

2.5 QCA Clocking

Because it synchronizes the function of many components, clocking is a crucial component of QCA circuit design.

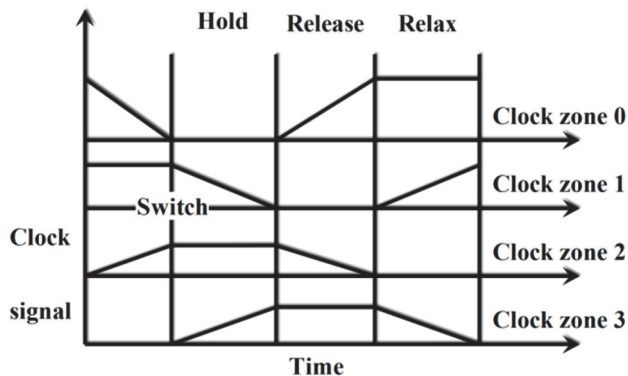


Figure 4 QCA clocking scheme

Clocking in QCA is achieved through the introduction of an external oscillating electric field as well as voltage pattern onto the circuit. By causing the quantum dots to alternate between their polarization states, this field enables logic operations to be precisely timed and synchronized. In order to provide dependable and synchronized computing in QCA circuits, proper clocking is essential. Fig. 4 depicts the phases of the QCA clocking scheme.

3 RELATED WORKS

Several advancements have been made in the development of QCA-based logic circuits, particularly focusing on optimizing XOR gate structures and their applications in arithmetic and cryptographic designs. A new logic circuit based on QCA was developed, incorporating a function generator using a newly designed XOR gate. This generator is capable of performing multiple logical tasks while occupying only 11.42 μm^2 and requiring nine clock cycles for operation [1]. Another study introduced a two-dot inverter cell, significantly reducing the cell count compared to traditional seven-dot designs. This compact inverter was utilized to build XOR gates and further extended to adder and subtractor circuits [2].

Practical XOR gate designs have also been evaluated for performance across various bit levels of arithmetic operations [3]. Some works have focused on optimizing MUX, flip-flop, and other logic gates to reduce the overall cell count and circuit area [4]. Novel XOR gate topologies have been proposed with minimal bridges and fewer cells, demonstrating benefits for communication-based applications, especially in encryption and decryption circuits [5, 6].

A multi-bit arithmetic logic unit (ALU) has been designed with fewer elements for logical and arithmetic operations, offering a simpler and more efficient structure [7]. An innovative MUX design was employed to construct logic gates and sequential circuits optimized for low-area applications [8]. Further studies focused on developing optimized parity generators and checkers using XOR gates for cryptographic applications [9]. Multi-bit full adders were implemented using majority gates, and new wire-crossing structures were proposed to reduce the number of dots and crossovers [10].

Minimal-cell XOR gates with simple layouts have been proposed as the basis for combinational circuits, including half adders, full adders, and parity checkers. Techniques for processor design, floor planning, and circuit simulation using QCA were also introduced [11]. Cryptographic circuit designs have been supported by fault-tolerant and scalable QCA structures, offering robustness for different bit sizes [12].

Reconfigurable QCA circuits have been proposed, offering benefits such as single-layer layouts and the elimination of coplanar wire-crossings. Some XOR gate designs require only 28 cells and occupy as little as 0.02 μm^2 , utilizing a single-layer structure without crossovers [13]. Reversible logic-based XOR gates have also been developed and employed in MUX designs, achieving significant cost reductions [14].

The use of two-cell inverters has been verified for half adder, full adder, and multi-bit adder circuits, leading to

substantial area savings [15]. A single-layer wire-crossing technique has also been proposed, eliminating the need for multiple cell types in layouts [16]. A fault-tolerant XOR structure with low area requirements has been introduced to ensure reliable operation in complex QCA systems [17]. Novel XOR gate designs that eliminate crossovers and noise have led to improved adder circuits, enhancing overall system performance [18].

Additional designs have employed coplanar techniques with single wire crossings, resulting in 19% cell count reduction and 6% savings in design overhead [19]. A convertible full adder-subtractor structure using a single layer and non-rotating cells showed improvements of 44%, 48%, and 36% in cell count, area, and energy dissipation respectively [20]. Furthermore, new reversible full adder designs have been proposed at both logic and layout levels, contributing to more efficient QCA circuit implementations [21].

Aamir Suhail Taray et al. [22] proposed a novel 3×3 universal and reversible logic gate (RLG-QCA) using the majority voter gate (MVA) approach implemented in QCA. The proposed achieves compact area of $0.0311 \mu\text{m}^2$ with a low latency of 0.5 clock cycles without any crossovers. R. V. Prasad Bhookya et al. [23] developed a hybrid full adder using Toffoli, Feynman, and Fredkin universal reversible logic gates in QCA technology. Angshuman Khan et al. [24] developed a multi-bit approximate full adder architecture called MAFA (RL) for low power application. The proposed design achieves 4% reduction in cell count and 13.3% lower clock phase usage compared to existing designs. A. Moustafa et al. [25] proposed optimized QCA designs for XOR, Half Adder, and Full Adder circuits, which were further extended to build Ripple Carry Adders (RCA) in 4-bit, 8-bit, and 16-bit versions. Hafeez et al. [26] focused on the development of fast adder layouts for nanotechnology applications using novel QCA-based design strategies.

4 PROPOSED METHOD

The Compact XOR gate is introduced in this section. Then, the proposed Compact XOR gate is used to design a novel full adders and half adders.

The selection of an 8-quantum dot XOR gate configuration is primarily motivated by various needs. It requires balanced complexity, area, and power efficiency within the QCA paradigm. XOR gates play a fundamental role in arithmetic and logical operations. The 8-QD configuration offers a compact and symmetric structure. It reduces the number of cells and interconnect delays compared to traditional multi-cell designs. In addition, the 8-QD layout simplifies the clocking zone arrangement and lowers switching energy. It is contributed to increased performance in terms of speed and power consumption.

The design of an XOR gate is important since it is a necessary component of many digital circuit applications. The output of a common logic gate called an XOR gate is false (0) when there are an even number of true inputs and true (1) when an odd number of true inputs occurs. The XOR gate expression is expressed as follows.

$$A \text{ XOR } B = A \oplus B = \bar{A}B + A\bar{B}$$

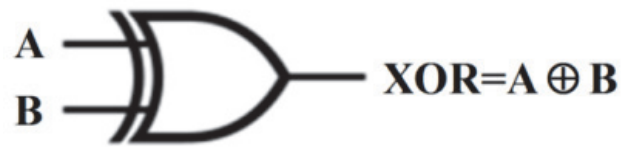


Figure 5 XOR gate

The symbol of XOR gate is shown in Fig. 5. Arithmetic operations, error detection, data comparison, and other logical processes all depend on the XOR gate's functionality. The promise of QCA technology is further enhanced by the creation of effective and optimized XOR gate designs, which also help to realize high-performance and low-area nanoscale computing systems.

Explicit interactions and half spacing between QCA cells are used in the suggested 2-input CompactXOR gate (shown in Fig. 6). Fig. 6 shows the architecture of our suggested 2-input QCA XOR gate, which only has 8 QCA cells. Interestingly, the Compact XOR gate only takes up $0.01 \mu\text{m}^2$ of space.

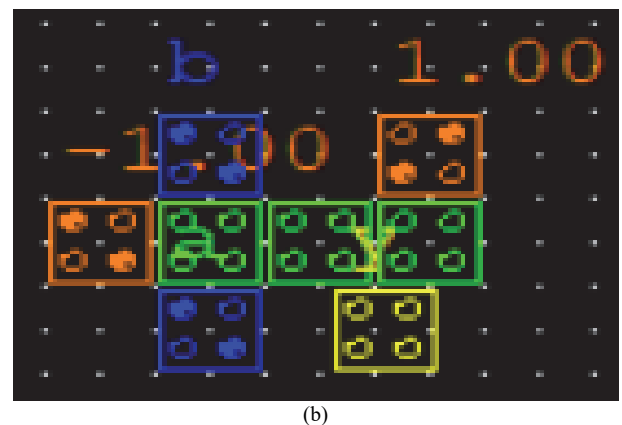
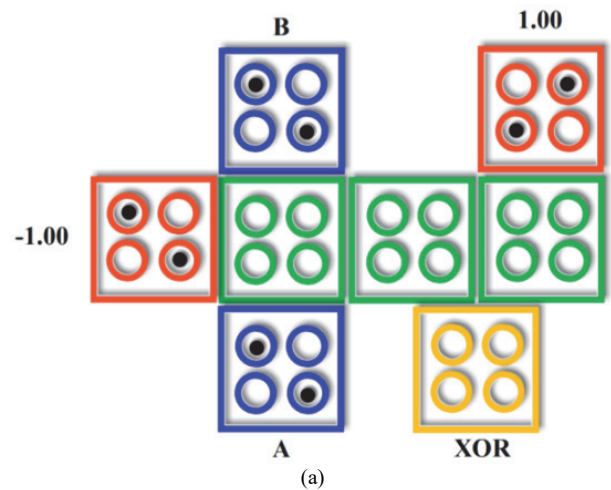


Figure 6 Proposed (a) schematic of compact XOR gate (b) QCA designer diagram of compact XOR gate

The proposed QCA half adder architecture.

This section presents HA architecture using the 2-input CompactXOR gate. The QCA HA is a basic component in digital circuits that computes binary addition on two input bits, generating the sum (S) and carry-out (Cout) outputs. It is widely used in arithmetic and logic operations.

The QCA half adder can be represented by the following equations: $S = A \oplus B$, $Cout = A \times B$. The logic diagram of HA is shown in Fig. 7.

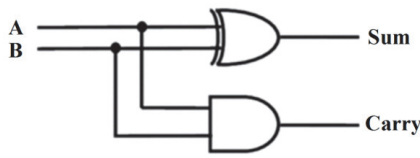
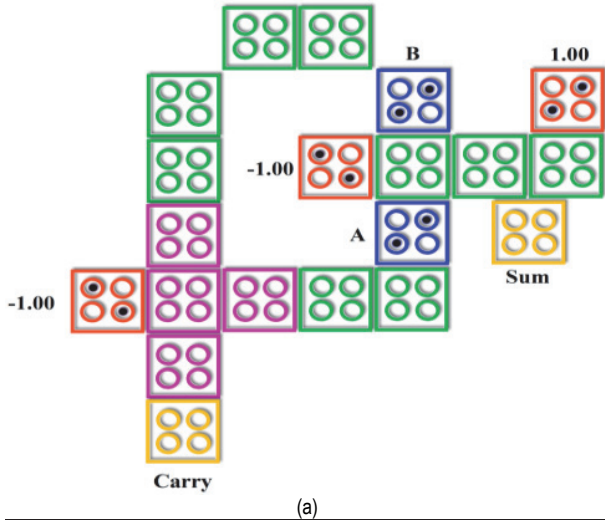


Figure 7 Logic diagram of HA

Fig. 8 shows the structure of QCA HA architecture, which uses 2-input Compact XOR gate.



(a)



(b)

Figure 8 Proposed HA structure (a) schematic (b) QCA designer

By using the proposed architecture, the QCA half adder proves improved performance characteristics such as reduced area overhead, minimized delay, and cross-over.

The proposed QCA-FA architecture:

The proposed QCA-FA architecture is explained in this section, using the 2-input Compact XOR gate. An FA is a critical component in digital circuits that performs the addition of three input bits and gives the sum and carry outputs. The performance of any digital system can be improved by integrating new FA designs.

The equations for the QCA full adder: $S = (A \oplus B) \oplus Cin$, $Cout = (A \times B) + (Cin \times (A \oplus B))$. The logic diagram of HA is shown in Fig. 9.

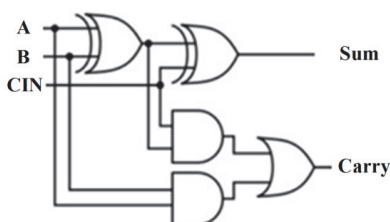
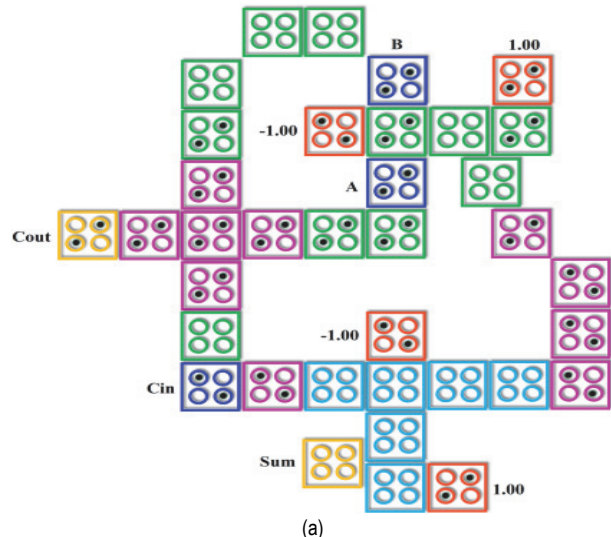


Figure 9 Logic diagram of FA

The proposed QCA full adder architecture based on the 2-input CompactXOR gate into its design, aiming to enhance its robustness, efficiency, and performance. Fig. 10 demonstrates the structure of the proposed QCA full adder architecture, showcasing the incorporation of the 2-input CompactXOR gate. This architecture provides proper generation of sum and carry-out outputs for different input combinations.



(a)



(b)

Figure 10 Proposed FA structure (a) schematic (b) QCA designer

The utilization of the proposed QCA full adder design model, with its integration of the 2-input CompactXOR gate, offers significant advantages in digital circuit design. It enables the development of high-performance systems with enhanced area efficiency, faster operation, and reduced power consumption.

The half-cell distance optimization in our design is based on minimizing signal interference and optimizing power efficiency within the QCA layout. This process involves systematically varying the inter-cell spacing and analyzing the resulting impact on signal integrity, polarization strength, and overall energy.

Specifically, we evaluated multiple half-cell distances within the operational limits and observed the polarization behavior and switching characteristics under different configurations. The optimal distance was selected based on the configuration that maintained maximum polarization stability with minimal energy dissipation. It is used for

reliable signal propagation across the circuit and reduces the overall footprint.

5 EXPERIMENTAL RESULTS

Our proposed work was executed using QCA Designer with the default parameters of a coherence vector simulation engine during the process of verification. The simulation was conducted using the parameters specified in Fig. 11. It specifies a total of 12800 samples to be used in the simulation with a convergence tolerance set at 0.001. The parameters related to the clock signal are defined as Clock High at 9.8×10^{-22} , Clock Low at 3.8×10^{-23} , and Clock Shift at 0.0×10^{000} , and the Clock Amplitude Factor is set to 2. The simulation also considers a Layer Separation of 11.5 and sets a Maximum Iterations Per Sample at 100000.

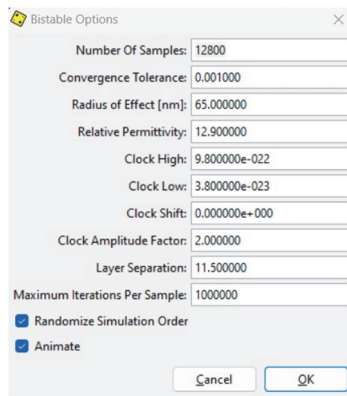
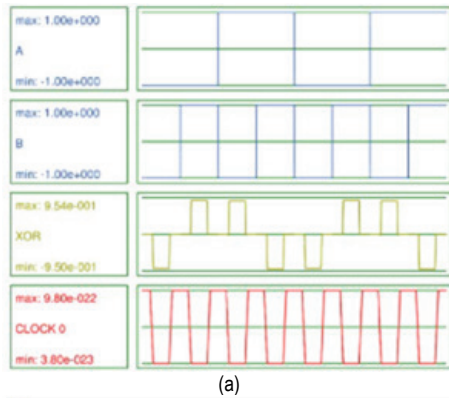
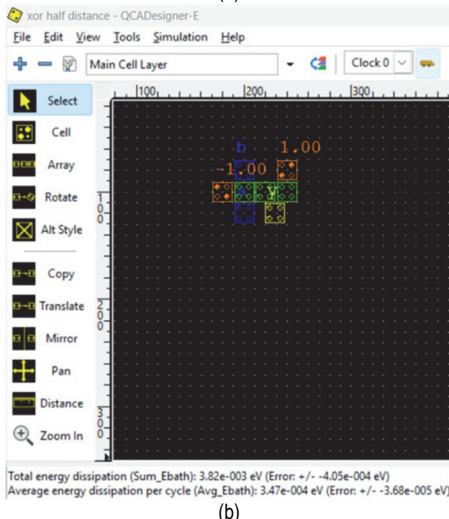


Figure 11 Parameter settings



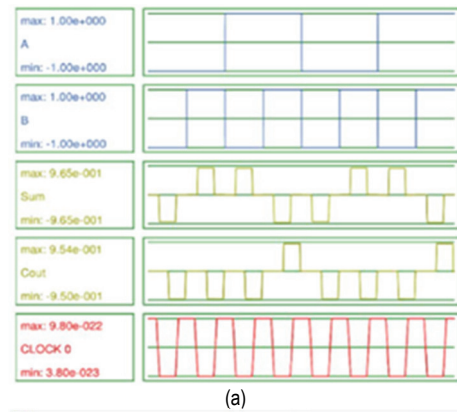
(a)



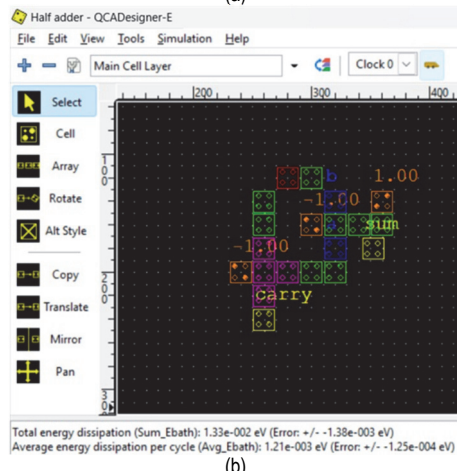
(b)

Figure 12 XOR gate (a) input and output waveform (b) energy dissipation

Simulation results of CompactXOR gate and average energy dissipation per cycle are shown in Fig. 12(a) and Fig. 12b. The input and output waveform of proposed HA and FA is shown in Fig. 13a and Fig. 14a. Similarly, the average energy dissipation per cycle for proposed HA and FA is shown in Fig. 13b and Fig. 14b, respectively. To validate the low-power characteristics of the proposed QCA-based arithmetic circuits, energy dissipation was analyzed using the MAUSPRITE simulation environment. The average energy dissipation per clock cycle was recorded as 3.47×10^{-4} eV for the XOR gate, 1.21×10^{-3} eV for the Half Adder, and 1.79×10^{-3} eV for the Full Adder. These values confirm the ultra-low power nature of the design when compared to conventional CMOS implementations and even to several recent QCA designs reported in literature.



(a)



(b)

Figure 13 HA (a) input and output waveform (b) energy dissipation

Tab. 1 provides the performance analysis of the suggested gate. In this case, CP stands for coplanar, ML for multi-layer, and NR for not necessary. Because of its unique features, the suggested Compact XOR gate design stands out when compared to other XOR gate designs. It accomplishes a very compact and efficient implementation with an extremely small size of $0.01 \mu\text{m}^2$ and only 8 QCA cells. The efficiency and simplicity of the suggested design are further enhanced by the fact that it executes logical operations without any crossings. With an exceptionally low latency of 0.25, the suggested Compact XOR gate in particular shows a markedly decreased operating delay. This suggests a quicker reaction and better performance in arithmetic and other applications where XOR operations are essential.

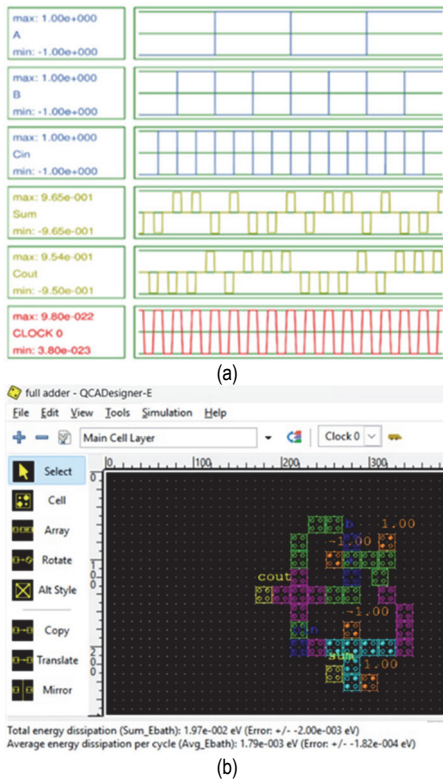


Figure 14 FA (a) input and output waveform (b) energy dissipation

Table 1 Performance evaluation of the suggested XOR gate

XOR	Area / μm^2	No of cells	Crossover types	Latency
V. C. Teja	0.22	121	CP	1
S. K. Lakshmi	0.07	64	ML	1
A. Shahidinejad	0.06	49	ML	1
H. S. Jagarlamudi	0.06	54	NR	0.75
M. R. Beigh	0.08	84	ML	1
M. Mustafa	0.09	55	NR	2
M. G. Waje	0.17	115	CP	1.5
M. Goswami	0.04	40	CP	0.75
S. Santra	0.08	51	CP	1.25
S. Santra	0.16	51	CP	1.25
M. Kianpour	0.05	47	CP	1
S.-H. Shin		71	NR	1.75
D. Ajitha	0.04	32	NR	3/4
M. T. Niemier	0.09	60	CP	1.5
S. Hashemi	0.08	54	CP	1.5
A. M. Chabi	0.03	29	NR	0.75
G. Singh	0.02	28	NR	0.75
A. M. Chabi	0.01	14	NR	0.5
Proposed CompactXOR gate	0.01	8	NR	0.25

The performance value of proposed HA is given in Tab. 2. In comparison to other designs, the proposed HA stands out due to its considerable amount of area and delay reductions. The HA design demonstrates an area efficiency of $0.02 \mu\text{m}^2$, requiring only 20 cells for implementation. This compact size indicates efficient space utilization and potential advantages in digital design.

Table 2 The Performance value of proposed HA

HA	Area / μm^2	No of cells	Crossover types	Latency
S. K. Lakshmi	0.08	77	ML	1
H. S. Jagarlamudi	NA	61	NR	0.75
S. Santra	NA	65	CP	1.25
S. Angizi	0.08	62	NR	2
D. Ajitha	0.05	34	NR	0.75
M. Poorhosseini	0.05	44	NR	1
Proposed HA	0.02	20	NR	0.25

Table 3 The Performance value of proposed FA

FA	Area / μm^2	No of cells	Crossover types	Latency
S. K. Lakshmi,	0.2	192	ML	2
F. Ahmad	0.15	120	CP	2.5
V. C. Teja	0.04	124	ML	1
S. Santra	0.28	150	CP	2.25
D. Ajitha	0.14	105	NR	1.25
T. N. Sasamal	0.04	49	CP	1
E. Taherkhani	0.28	228	NR	1.75
P. Kumari	0.37	221	CP	2
M. Sarvaghad	0.04	46	NR	0.75
Proposed FA	0.04	36	NR	0.75

The value of proposed FA is given in Tab. 3. In comparison to other designs, the proposed FA design achieves area reductions considerably. The FA design achieves an area efficiency of $0.04 \mu\text{m}^2$, utilizing only 36 cells for implementation. Also, another advantage of the proposed FA design is its low latency of 0.75. This signifies a relatively fast operation in addition.

The proposed QCA-based design shows enormous potential for real-world applications due to its nanoscale footprint, low power consumption and high-speed switching. It is suitable for next-generation processors and cryptographic hardware where compactness and security are critical. In medical electronics and IoT devices, the energy-efficient nature supports extended battery life. Additionally, its minimal energy profile is ideal for environmental sensing and automation systems in remote locations.

6 CONCLUSION

This study presents an efficient and compact Quantum-dot Cellular Automata (QCA) design for implementing Half Adder (HA) and Full Adder (FA) circuits utilizing a newly proposed XOR gate structure. The novel XOR gate, composed of only 8 quantum dots, enables significant reductions in area, complexity, and latency when compared to traditional QCA-based implementations. The proposed design emphasizes optimized cell-to-cell interactions and uses the concept of half-distance placement, thereby increasing signal integrity and reducing crossover requirements. Overall, the proposed QCA-based HA and FA designs represent a promising advancement in the field of nanoscale digital circuit design.

7 REFERENCES

- [1] Sakthivel, B. & Padma, A. (2020). Area and delay efficient GDI based accuracy configurable adder design. *Microprocessors and Microsystems*, 73, 102958. <https://doi.org/10.1016/j.micpro.2019.102958>
- [2] Shahidinejad, A. & Selamat, A. (2012). Design of first adder/subtractor using quantum-dot cellular automata. *Advanced Materials Research*, 403, 3392-3397. <https://doi.org/10.4028/www.scientific.net/AMR.403-408.3392>
- [3] Kumar, R. & Ranjan, P. (2024). Quantum-Dot Cellular Automata Based Arithmetic Operations for Low-Power Computing. *International Journal of Electronics*, 111(5), 765-781.
- [4] Saminathan, S., Ponniah, R., Muthurathnam, K., & Somasundaram, K. (2023). Internet of Things based reconfigurable SIMD processor for high-speed end devices

- in FPGA. *Tehnički Vjesnik - Technical Gazette*, 30(6), 1975-1981. <https://doi.org/10.17559/TV-20230404000502>
- [5] Beigh, M. R., Mustafa, M., & Ahmad, F. (2013). Performance evaluation of efficient XOR structures in quantum-dot cellular automata (QCA). *Circuits and Systems*, 4(2), 147-156. <https://doi.org/10.4236/cs.2013.42021>
- [6] Aljanabi, W. & Albayrak, M. (2018). Design and implementation of 4-bit quaternary MVL arithmetic and logic unit. *Tehnički Vjesnik - Technical Gazette*, 25(2), 330-338. <https://doi.org/10.17559/TV-20170210143503>
- [7] Patel, R. & Shukla, V. (2024). Quantum-Dot Cellular Automata (QCA) for Low-Power Arithmetic Circuits: A Survey and Novel Design Proposals. *Journal of Semiconductor Technology and Science*, 24(2), 105-118.
- [8] Sahu, S. & Chatterjee, S. (2023). Design and Optimization of a Compact XOR Gate for QCA-Based Full Adder Circuits. *Nano-Micro Letters*, 15(4), 272-283.
- [9] Zhang, Q. & Liu, X. (2023). Low-Power Quantum-Dot Cellular Automata Half-Adder Design for Nanoelectronics. *Journal of Nanoelectronics and Optoelectronics*, 18(1), 52-60.
- [10] Kianpour, M., Sabbaghi-Nadooshan, R., & Navi, K. (2014). A novel design of 8-bit adder/subtractor by quantum-dot cellular automata. *Journal of Computer and System Sciences*, 80(7), 1404-1414. <https://doi.org/10.1016/j.jcss.2014.04.008>
- [11] Shin, S. H., Jeon, J. C., & Yoo, K. Y. (2014). Design of wire-crossing technique based on difference of cell state in quantum-dot cellular automata. *International Journal of Control and Automation*, 7(4), 153-164. <https://doi.org/10.14257/ijca.2014.7.4.14>
- [12] Ajitha, D., Ramanaiyah, K. V., & Sumalatha, V. (2015). An efficient design of XOR gate and its applications using QCA. *i-Manager's Journal on Electronics Engineering*, 5(3), 22-29. <https://doi.org/10.26634/ijee.5.3.3394>
- [13] Hashemi, S., Farazkish, R., & Navi, K. (2013). New quantum dot cellular automata cell arrangements. *Journal of Computational and Theoretical Nanoscience*, 10(4), 798-809. <https://doi.org/10.1166/jctn.2013.2773>
- [14] Chabi, A. M., Sayedsalehi, S., Angizi, S., & Navi, K. (2014). Efficient QCA exclusive-or and multiplexer circuits based on a nanoelectronic-compatible designing approach. *International Scholarly Research Notices*, 2014, 463967. <https://doi.org/10.1155/2014/463967>
- [15] Singh, G., Sarin, R. K., & Raj, B. (2016). A novel robust exclusive-OR function implementation in QCA nanotechnology with energy dissipation analysis. *Journal of Computational Electronics*, 15(2), 455-465. <https://doi.org/10.1007/s10825-016-0804-7>
- [16] Chabi, A. M., Roohi, A., Khademolhosseini, H., Sheikhaal, S., Angizi, S., Navi, K., & DeMara, R. F. (2017). Towards ultra-efficient QCA reversible circuits. *Microprocessors and Microsystems*, 49, 127-138. <https://doi.org/10.1016/j.micpro.2016.09.015>
- [17] Lakshmi, S. K. & Athisha, G. (2011). Design and analysis of adders using nanotechnology based quantum dot cellular automata. *Journal of Computer Science*, 7(7), 1072-1077. <https://doi.org/10.3844/jcssp.2011.1072.1079>
- [18] Angizi, S., Alkaldy, E., Bagherzadeh, N., & Navi, K. (2014). Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. *Journal of Low Power Electronics*, 10(2), 259-271. <https://doi.org/10.1166/jolpe.2014.1321>
- [19] Poorhosseini, M. & Hejazi, A. R. (2018). A fault-tolerant and efficient XOR structure for modular design of complex QCA circuits. *Journal of Circuits, Systems and Computers*, 27(07), 1850115. <https://doi.org/10.1142/S0218126618501153>
- [20] Ahmad, F., Bhat, G. M., & Ahmad, P. Z. (2014). Novel adder circuits based on quantum-dot cellular automata (QCA). *Circuits and Systems*, 5(6), 142-152. <https://doi.org/10.4236/cs.2014.56015>
- [21] Sasamal, T. N., Singh, A. K., & Mohan, A. (2016). An optimal design of full adder based on 5-input majority gate in coplanar quantum-dot cellular automata. *Optik*, 127(20), 8576-8591. <https://doi.org/10.1016/j.ijleo.2016.06.014>
- [22] Taray, A. S., Singh, S. K., Singh, Y., Naaz, F., & Hazra, P. (2024). Design and power optimization of a QCA-based universal reversible logic gate architecture using cell interaction approach. *Microelectronics Reliability*, 159, 115446. <https://doi.org/10.1016/j.microrel.2024.115446>
- [23] Bhookya, R. V. P. & Ravindra, J. V. R. (2024). Design of high speed hybrid full adder using reversible logic gates. *AIP Conference Proceedings*, 2942, 020017. <https://doi.org/10.1063/5.0196570>
- [24] Khan, A., Parameshwara, M. C., & Maroof, N. (2024). Reconfigurable lower-part approximate adder with error-tolerant application: An approach using QCA computing. *International Journal of Ad Hoc and Ubiquitous Computing*, 46(2), 65-79. <https://doi.org/10.1504/IJAHUC.2024.138749>
- [25] Singh, H. & Bhattacharya, A. (2024). Efficient Quantum-Dot Cellular Automata Based Arithmetic Circuits: Design, Optimization, and Performance Evaluation. *International Journal of Nanoelectronics and Materials*, 18(3), 131-146.
- [26] Hafeez, T., Bilal, B., & Malik, B. A. (2025). Optimization of fast adders in quantum dot cellular automata nanotechnology. *Journal of the Institution of Engineers (India): Series B*. <https://doi.org/10.1007/s40031-025-01235-y>

Contact information:**V. BHUVANESWARI**

(Corresponding author)
Department of ECE, SRM Institute of Science and Technology,
City Campus, Vadapalani, Chennai, Tamil Nadu, India
E-mail: bhuvanasmist@gmail.com

S. YUVARAJ

Department of ECE, SRM Institute of Science and Technology,
SRM Nagar, Kattankulathur, Chennai, Tamil Nadu, India