ISSN 1330-3651 (Print), ISSN 1848-6339 (Online) https://doi.org/10.17559/TV-20250103002232
Original scientific paper

Hybrid Swarm Intelligence for FPGA-Based Noise Mitigation in Gradient-Sensitive MRI Systems

Nirmala R, Senthilkumar V M, Malathi M, Vinoth Kumar K*

Abstract: This research presents an advanced Magnetic Resonance Imaging (MRI) signal processing framework to address time-varying noise and environmental disturbances. A novel adaptive filtering mechanism is proposed to enhance noise mitigation while dynamically adjusting coefficients based on gradient field variations and magnetic coil responses. The core contribution lies in the development of a Modified Opposition-Based Artificial Ant Colony Optimization (MOACO) algorithm, marking the first application of an optimization algorithm tailored for MRI systems. The proposed method integrates swarm intelligence by combining opposition-based ant bee colony optimization, leveraging the cooperative behaviors of ants and bees to optimize the adaptive filter's weight estimation. The optimization process dynamically adjusts the step size, ensuring faster convergence and improved noise suppression. A Parallel Architecture Opposition-Based ABC algorithm is introduced for efficient hardware implementation. The effectiveness of the proposed solution is evaluated against conventional filtering methods, including Two-Dimensional LMS (TDLMS), Recursive Least Squares (RLS), and Adaptive Filtering Least Mean Error (AFLME). The algorithms are implemented on a Field-Programmable Gate Array (FPGA) platform, specifically the EP-FPGA-256C6 Cyclone, utilizing 65 nm and 90 nm CMOS technology nodes to ensure optimal power efficiency, reduced Look-Up Table (LUT) utilization, and minimal delay. Experimental results demonstrate that the MOACO-enhanced adaptive filtering framework significantly improves power efficiency, circuit performance, and noise reduction, leading to enhanced MRI image reconstruction and minimized motion artifacts. This study establishes a novel direction for integrating AI-driven optimization techniques with hardware-based MRI signal processing, paving the way for more efficient medical imaging systems.

Keywords: adaptive filtering; artificial ant colony optimization; FPGA implementation; gradient-based optimization; MRI signal processing

1 INTRODUCTION

The high-resolution MRI scanning system uses high throughput controllers, superconducting magnetic coils, gradient field coils, radio frequency coils as main units. Apart from this the system has analog signal processing, filtering units and reconstruction blocks. The system is highly complex in design and functions. The magnetic and radiofrequency signals make the scanning accurate. Still the system needs to achieve high signal to-noise ratio (SNR). Through proper circuit elements the contrast-to-noise ratio (CNR) can be improved. Even though signal averaging improves the quality of k-space, the acquiring time has some limitations on performing the averaging of information. The pulse sequence and acquisition parameters are optimized to reduce the noise power. This improves the SNR and CNR of the system. Adaptive filters can be employed for filtering of images. In the past, adaptive filters were designed for feature extraction and denoising of ECG signals [1-3]. Adaptive filtering techniques like the least mean squared (LMS) algorithm, recursive least square algorithm were easy to implement but suffer from the convergence behavior. When compared to linear filtering, the window size is to be varied so as to update the filter weights. The adaptive filters were used in MRI systems to remove the noises in the acquisition unit. The weight updates are done in average mode in filters like Two Dimentional Average LMS algorithm. The least mean estimates were also used in adaptive filter [4-6].

In MRI image reconstruction, sequence control is the important block which will control the timing of various gradient fields. For the acquisition of image, the radio frequency was transmitted by the circuit. The gradients signals were applied in synchronous manner and the resonance signal is recorded. The timing of each RF and gradient application process is properly done for each slice of the human organ. The unwanted anatomical motions are discarded This can be done by controlling the radio frequency receiver. The electrodes placed in the patients are prone to noises and unwanted artifacts. The MRI acquisition unit is also affected by the noises. [7-10].

2 LITERATURE REVIEW

The MRI acquisition unit uses low power, high speed adaptive filters for noise removal. The circuit should be designed to eliminate the noises and needs adaptation based on envirоinment noises [11-13]. Swarm-based optimization uses natural and self-organization algorithms. The adaptive filter is used for edge detection even in high noise intensity. The filter is suitable for low power applications. However, the algorithm is bulky in implementation and switches between filtering. Sparse system identification using adaptive Proportionate-type normalized LMS filter is implemented for echo cancellation. Hardware implementation of LMS adaptive filter needs a large number of multipliers but the components can be reduced using the approximate arthmetic units. The LMS filters were implemented using approximate arithmetic circuits which consumed less power. Filter circuits for communication need to work in high frequency with good current driving capability.

For noise and artifact removal Delayed Least Mean Square (DLMS) algorithm was implemented. Machine learning methods were implemented by combining the features of frequency-domain for noise removal through adaptive filter. Deep neural network was used for the optimization. An integrated adaptive filtering algorithms with deep learning method uses differentiable layer. Weight Optimization was used on Adaptive filtering algorithms. The optimization system used algorithms like LMS and RLS. Fast and higher order filter was developed. The circuit does not use any clock for control [14-16]. For high frequency, the adaptation is done with minimum error. The system identification was investigated using LMS adaptive filter. AF tracking and systems identification were done using various algorithms [17-19]. The design was

implemented for echo cancellations. The weights of the filter are updated with the DNN algorithms. Several intelligence and optimization methods were used. Sparse representations using compressive sensing were done. The super pixel algorithm was applied for image reconstruction in group sparsity method. The method was regularized for data sample choices. Still artificial intelligence and nature computing are found useful in the compressed sensing when distributed computing is involved. The Grey Wolf Optimizer Algorithm was applied in the computing for optimization. The functions were optimized with the modified Grey Wolf algorithm [20-22]. The FPGA design is scalable to larger MRI system by increasing the Fast Fourier transform FFT size. The image reconstruction can be done using higher computation unit available in the FPGA [23]. The methods in the past which were involved in disease diagnosis [24] used FFT algorithm for self supervised learning. Considering the deep space-time-coil reconstruction network for larger MRI system modular design and optimized resource allocation can be done [25-27].

The current integrated circuits used in MRI analysis are less efficient and are affected by instrumentation noise. This research focuses on improving Magnetic Resonance Imaging (MRI) systems by addressing the challenges posed by time-varying noise and environmental disturbances. Since MRI unit is capable of processing multiple signals the challenge is on filtering the noise in all channels. There is a research gap or not yet implemented swarm intelligence method in MRI circuit units. Conventional FPGA systems provide only noise filters which are bulky and need more computation to perform filtering.

3 PROPOSED METHODOLOGY

The main problem in MRI imaging is that the bandwidth of noise is wide and it changes for every slice in MRI scanning. The k-Space has individual RF signal. The adaptive filter weights have to be updated based on the noise bandwidth changes. For example in this type of non-invasive diagnostic method, the patient is sent into varying radio frequency and magnetic field, the nuclei generates a resonant frequency which is recorded. Since the cardiac monitoring system runs parallel to the imaging process, the electrocardiographic signals are superimposed by the noise due to the changing magnetic fields. Observing the resonance signal, the gradient and RF pulses were managed by the Control unit. The process steps of opposition based ADC are shown in Fig. 1.

Very large integrated circuits have played important role in the design of filters for Magnetic resonance imaging (MRI) applications. In this radiological equipment, the adaptive filter is designed the images are to be reconstructed using hardware unit. The images have large temporal and spatial resolution. The image slices were more and is often affected by background noises. Large number of MRI slices were used for image acquisition. In single-shot echo-planar imaging (EPI) the sequences were acquired through fast gradient switching. Acoustic noise, eddy current noise, were affecting the image clarity. The motion in subjects causes image offset wandering noise which could cause drift in frequency. The magnetic field fluctuations and RF acquisition can cause intensity and geometric distortions. The acquisition hardware processes the images with high resolution, gain and less noise. The hardware units consist of the active and passive circuits which process the acquired information so the gain and noise rejection ratio are higher. The circuit has resonant frequency monitoring and eddy current compensation.

Some of the optimization algorithms used in other areas were Ant Colony Optimization (ACO), Particle Swarm Optimization (PSO) and Bee Colony Optimization (BCO) algorithms. In this work for the first time an optimization algorithm for MRI application is developed. An opposition-based ant bee colony method is developed. The method combines the Swarm behavior of bees and ant in the same algorithm. The weight estimation of the adaptive filter based on step size is optimized. The step size determines the convergence behavior where in this work the swarm-based optimization takes care of this. Considering the optimization problems the bee algorithm updates the position of the bee with respect to the food and hives. The hardware implementation of the update bee position is shown in Fig. 4. The blocks involved are adders, multipliers, comparator and buffers. The subtractor is implemented using the adder and complement units.

The Opposition-Based Artificial Bee Colony (OABC) algorithm in parallel architecture for hardware implementation is presented in Fig. 2. This approach enhances computational efficiency by leveraging a Finite State Machine (FSM)-based sequential unit that orchestrates the execution steps of the OABC algorithm. The entire process is implemented in VHDL, ensuring hardware-level optimization and seamless execution. At the core of the system, a register bank is used to store the bee's position, which is generated using a Random Number Generator (RNG). The key role of the register bank is to maintain and update the bee positions dynamically as the algorithm progresses. The optimization process begins with identifying a neighbor (k) and its associated parameter, which is refined iteratively. The S parallel bees act as inputs from the RNG, ensuring diverse and efficient exploration of the solution space.

A crucial design aspect is the sharing of hardware resources in a multiplexed mode, which significantly reduces the implementation cost. This resource-sharing strategy enhances efficiency by allowing multiple processing units to operate in parallel without increasing hardware overhead. During each execution stage, the fitness function is continuously evaluated and updated based on the bee positions. This ensures that the solution converges toward optimal values with minimal computational delay. The evaluation and comparison of the fitness function are performed using dedicated processing elements, such as comparators. These comparators assess the updated values and determine whether a new position should be adopted based on fitness improvements. The results of these computations are then stored in an inbuilt latch, ensuring that intermediate results are preserved for subsequent iterations.

To enhance current driving capability, the stored values are amplified using buffer stages. These buffers strengthen the signal integrity and prevent degradation during transmission across different hardware components. The implementation of this parallelized OABC

architecture in VHDL enables efficient execution, low power consumption, and improved optimization accuracy. This hardware-centric approach to swarm intelligence optimization marks a significant advancement in computational performance, particularly in real-time applications where speed and efficiency are critical. By integrating FSM-based control with parallel processing units, the system effectively balances speed, accuracy, and resource utilization, making it highly suitable for high-performance computing applications.

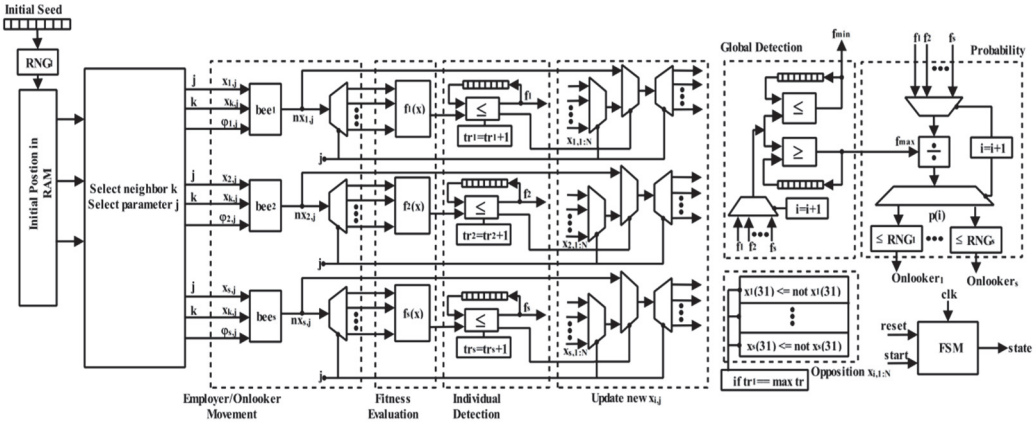
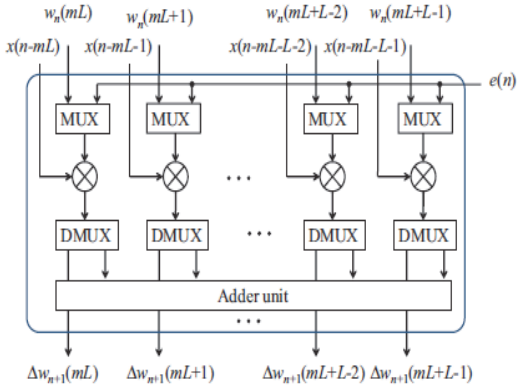
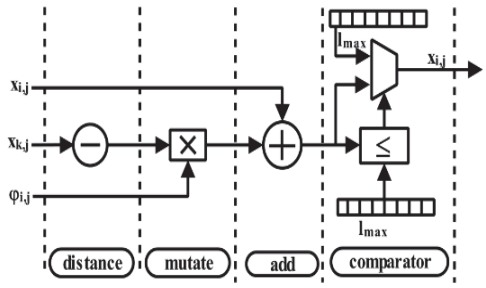


Figure 1 The Opposition-based ABC architecture

By this the bee position is improved so it can reach the hive quickly. The global fitness value and the bee positions were updated in the LUT. The requirement of LUT is varied from device to device. In this work for the analysis of devices, the algorithms were implemented in various devices. Through continuous trials the bee positions are determined in conventional methods but in the proposed method the trials are optimized using the adaptive methods so the convergence behaviors improve and the results are obtained quickly. Here Newton-Raphson algorithm is used for the computation of probabilities. By this the onlooker bees find the food sources correctly. Poor sources are eliminated so the time is saved. Only the food sources with rich quantity are chosen.



a) Processing element architecture



b) Update architecture of bee position unit

Figure 2 The Opposition-Based Artificial Bee Colony (OABC) algorithm in parallel architecture for hardware implementation

The processing element architecture is shown in Fig 2a. It consists of mux unit and demux unit to select the input and output. Multiplier unit is to perform all computation.

Fig. 2b shows the bee position update architecture. The circuits have sequential processing structure. The circuits were implemented and executing each occupying different LUTs. In convention digital processing units the adaptive filter takes more time for convergence and the stability is low due to the limitation of internal cache availability. But in FPGA due to the flexibility in the Finite State Machine (FSM) controlled process, the convergence rate can be improved.

The implemented structure for the error computation block functions faster for clock frequency of 500-800 Hz. The FIR based design generates the error signals from the difference of the filter output and the desired signal. The critical path is optimized using the adder by reducing stages to log2 *N*. and thus improves the critical path.The automatic updating of weights for the filters is done using the swarm design which operates in a way to optimize the weights based on the error output. The adaptive algorithm updates the weights using hardware blocks like $N + 1$ taps multipliers.

4 RESULTS AND DISCUSSION

The VHDL Implementation of all processing elements was done in Quartus software.

The following parameters were analyzed:

a. The thermal power dissipation - Dissipated power.

b. I/O power due to ports, drivers and capacitive load switching.

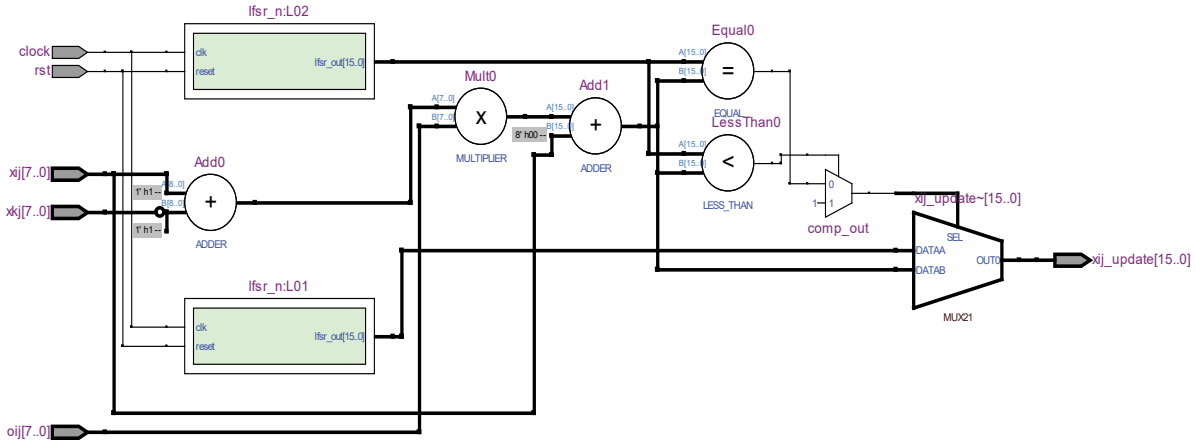
c. Dynamic power dissipation: Measure of power consumed by the switching activities of active transistors and load capacitance switching.

d. CDPD - Core Dynamic Power Dissipation of internal core components capacitance and resistance.

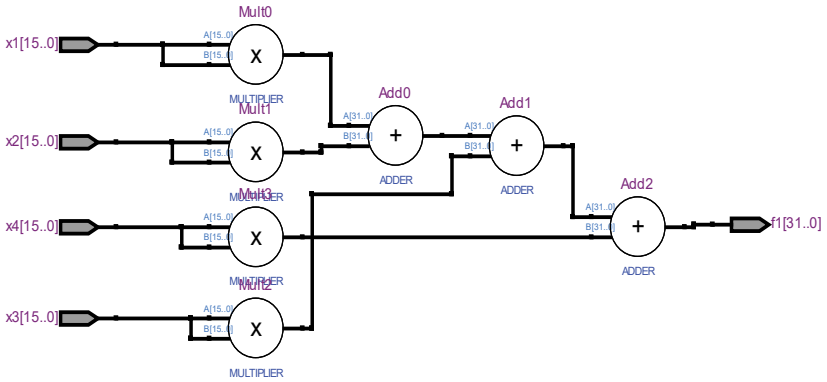
e. CSPD - Core Static power Dissipation is the power consumed in idle state. There will be leakage currents at low power technologies.

The RTL view of the building blocks of the proposed system is shown in Fig. 3a to Fig. 3d. The complete RTL view of the proposed system is shown in Fig. 4.

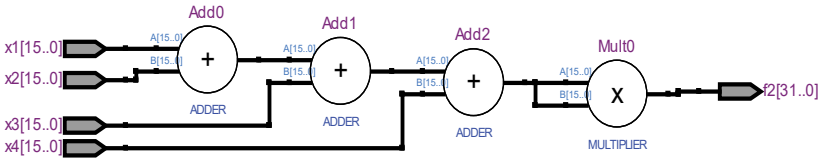
The ACO algorithm main component is the fitness function. The optimization of the adaptive filter algorithm is determined by the fitness function. The performance of the fitness function with respect to power, LUT and delay is shown in Tab. 1 to Tab. 3.



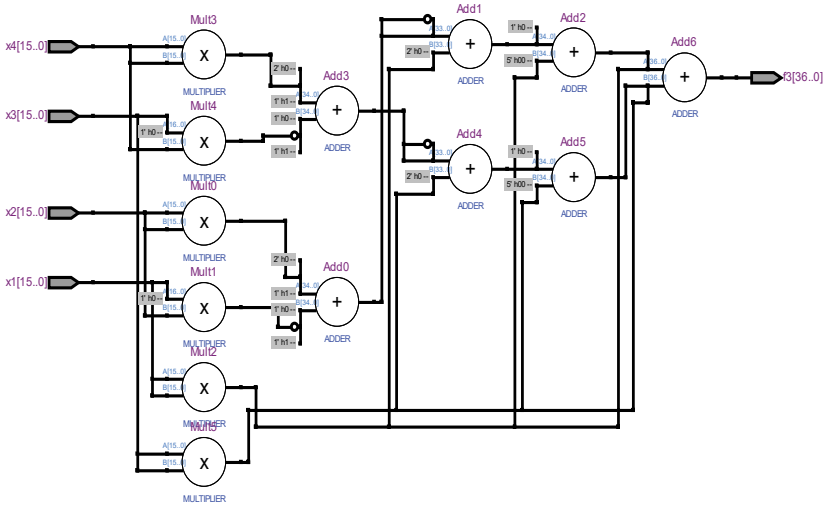
a) RTL view of architecture for updating the bee position



b) RTL view of architecture for function f1(x)



c) RTL view of architecture for function f2(x)



d) RTL view of Architecture for function fs(x)

Figure 3 The RTL view of the building blocks of the proposed system

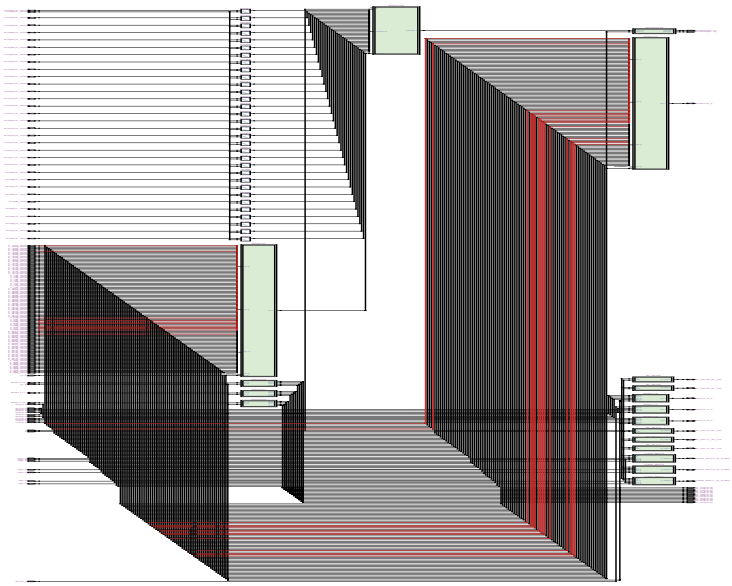


Figure 4 RTL view of architecture for proposed architecture

From Tab. 1 to Tab. 3 above it can be observed that the FPGA device EP-FPGA-256C6 cyclone 3 gives better performance compared to other devices. So the work is implemented in this device for the rest of the implementation. The LUT provides the information of the area of the circuits. The delay gives the speed of operation and the power dissipation confirms the low power operation. This enables to develop the product as a battery-operated device if applied to other systems. But in MRI since there are dedicated power units, battery is not required. But if the proposed is implemented for other applications, the battery usage is an important parameter. The Tab. 1 to Tab. 3 show the performance of various units

Table 1 Parameter LUT and delay analysis of updated bee position

Device	LUT			Delay / nS	Power Dissipation / mW			
	Available	Used	Utilization / %		CDPD	CSPD	ITPD	TTPD
EP-FPGA-256C5	4608	74	2	14.871	26.64	27.27	124.82	178.73
EP-FPGA-256C6	5136	72	1	13.242	19.6	56.19	67.45	143.24
EP-FPGA-484C3	12480	61	< 1	12.156	45.27	405.34	122.31	572.92
EP-FPGA-484C2	38000	61	< 1	13.524	42.07	402.35	97.31	541.73

Table 2 Parameter analysis-power dissipation of proposed algorithm

FPGA Family	Device	Power Dissipation / mW			
		Core Dynamic Power Dissipation	Core Static Power Dissipation	I/O Thermal Power Dissipation	Total Thermal Power Dissipation
Cyclone II	EP-FPGA-256C5	343.54	167.99	1087.55	1599.08
Cyclone III	EP-FPGA-256C6	148.66	96.04	498.67	743.37
Stratix II	EP-FPGA-484C3	250.47	417.61	617.02	1285.1
Stratix III	EP-FPGA-484C2	238.50	402.39	568.69	1209.58

Table 3 Proposed method analysis

FPGA Family	Device	LUT			Delay / nS
		Available	Used	Utilization / %	
Cyclone II	EP-FPGA-256C5	4608	1584	34	29.255
Cyclone III	EP-FPGA-256C6	5136	1701	33	22.562
Stratix II	EP-FPGA-484C3	12480	1391	1	16.584
Stratix III	EP-FPGA-484C2	38000	1402	< 1	18.160

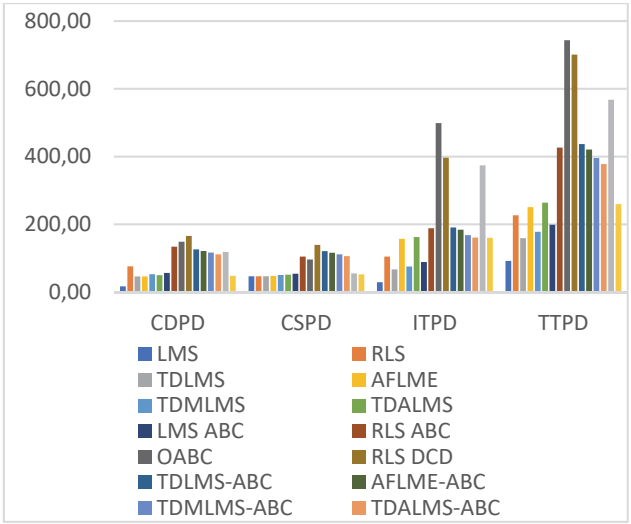


Figure 5 Performance of various parameters for different filters

Fig. 5 shows the comparison chart of various algorithms implemented for filters. The design has a gradient signal complexity management during real-time operation. The ACO algorithm main component is the fitness function. The optimization of the adaptive filter algorithm is determined by the fitness function. The global fitness value and the bee positions were updated in the LUT as per the real time operation. The weight estimation of the adaptive filter based on step size is optimized according to

the real time operation. The step size determines the convergence behavior where in real time adaptive filter with swarm-based optimization takes care of this.

Considering the optimization problems the bee algorithm updates the position of the bee with respect to the changes in the real time data. In modular design, reusable units for even 1024 point FFT can be designed and called for each voxel of MRI reconstruction process. This will enhance the usage of LUTs within the system. As the proposed design is for 65 nm the speed is also higher with low power operation. The processing units like multipliers, adders, buffers, logic blocks, memory, and interconnects can be scalable. To further increase the FPGA scalability the proposed design can be combined with the high-bandwidth memory (HBM) or hybrid memory cubes (HMCs) to improve the operation and scalability.

5 CONCLUSION

This paper presents the implementation of FPGA system for MRI analysis. In this work for the first time an optimization algorithm for MRI application is developed. An opposition-based ant bee colony method is developed. The method combines the Swarm behavior of bees and ants in the same algorithm. The weight estimation of the adaptive filter based on step size is optimized. The step size determines the convergence behavior where in this work the swarm-based optimization takes care of this. The implemented structure for the error computation block functions faster for clock frequency of 500-800 Hz. The FIR based design generates the error signals from the difference of the filter output and the desired signal. The critical path is optimized using the adder by reducing stages to log2 *N*. and thus improves the critical path. Modified Opposition-Based Artificial Ant Colony Optimization (MOACO) algorithm is superior when compared to the previous methods. For implementation Quartus software is used.

In future ASIC will be implemented to accomodate both analog and digital units of filtering. In addition AI based methods will be implemented for signal processing of MRI signals.

6 REFERENCES

[1] Kaya, Z. & Seke, E. (2020). A novel addressing algorithm of radix-2 FFT using single-bank dual-port memory. *Circuit World*, *48*(1), 64-70. https://doi.org/10.1108/CW-06-2020-0108

[2] Senthilkumar, V. M., Kalaiselvi, K., Umadevi, K., & Vinoth Kumar, K. (2025). Performance enhanced Penta-MTJ based logic gates using FinFET for low power and high-speed applications. *Tehnički vjesnik*, *32*(5), 1896-1901. https://doi.org/10.17559/TV-20250103002231

[3] Zhao, Y., Lv, H., Li, J., & Zhu, L. (2022). High performance and resource efficient FFT processor based on CORDIC algorithm. *EURASIP Journal on Advances in Signal Processing*, *2022*(1), 1-14. https://doi.org/10.1186/s13634-022-00855-6

[4] Jian, W., Xianbin, L., Guangteng, F., & Zhouhui, T. (2019). A Parallel Radix-2k FFT Processor using Single-Port Merged-Bank Memory. *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 1-5. https://doi.org/10.1109/ISCAS.2019.8702580

[5] Liu, S. & Liu, D. (2018). Design Space Exploration of 1-D FFT Processor. *Journal of Signal Processing Systems*, *90*(11), 1609-1621. https://doi.org/10.1007/s11265-018-1371-x

[6] Ma, Z., Yin, X., & Yu, F. (2015). A Novel Memory-Based FFT Architecture for Real-Valued Signals Based on a Radix-2 Decimation-In-Frequency Algorithm. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *62*(9), 876-880. https://doi.org/10.1109/TCSII.2015.2433531

[7] Wang, J., Li, S., & Li, X. (2020). Scheduling of Data Access for the Radix-2k FFT Processor Using Single-Port Memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *28*(8), 1676-1689. https://doi.org/10.1109/TVLSI.2020.2992021

[8] Garrido, M., Sánchez, M. A., Vallejo, M. L. L., & Grajal, J. (2017). A 4096-Point Radix-4 Memory-Based FFT Using DSP Slices. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *25*(1), 375-379. https://doi.org/10.1109/TVLSI.2016.2567784

[9] Senthilkumar, V. M., Nirmala, R., Satish Kumar, R., & Vinoth Kumar, K. (2025). Enhanced low power FinFET-based flash ADC design for high-speed electronics applications. *Technical Gazette*, *32*(2), 466-473. https://doi.org/10.17559/TV-20240801001895

[10] Sadaghiani, A. K., Sheikhaei, S., & Forouzandeh, B. (2022). Low Complexity Multiplierless Welch Estimator Based on Memory-Based FFT. *Journal of Circuits, Systems and Computers*, *31*(15), 2250215. https://doi.org/10.1142/S0218126622200031

[11] Senthilkumar, V. M., Muruganandham, A., Ravindrakumar, S., & Ganesh, N. S. G. (2019). FINFET operational amplifier with low offset noise and high immunity to electromagnetic interference. *Microprocessors and Microsystems*, *71*, 102887. https://doi.org/10.1016/j.micpro.2019.102887

[12] Guo, Y., Wang, Z., Hong, Q., Luo, H., Qiu, X., & Liang, L. (2023). A 60-Mode High-Throughput Parallel-Processing FFT Processor for 5G/4G Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *31*(2), 219-232. https://doi.org/10.1109/TVLSI.2022.3227346

[13] Wang, J., Liu, Y., Zhang, W., & Li, K. (2014). Compressed Sensing Image Reconstruction Based on Improved Particle Swarm Optimization Algorithm. *Applied Mechanics and Materials*, *599-601*, 1453-1456. https://doi.org/10.4028/www.scientific.net/AMM.599-601.1453

[14] Wang, Q., Li, D., & Shen, Y. (2017). Intelligent nonconvex compressive sensing using prior information for image reconstruction by sparse representation. *Neurocomputing*, *224*, 71-81. https://doi.org/10.1016/j.neucom.2016.10.060

[15] Yu, H., Jiang, M., Chen, H., Feng, J., Wang, Y., & Lu, Y. (2017). Super-pixel algorithm and group sparsity regularization method for compressed sensing MR image reconstruction. *Optik*, *140*, 392-404. https://doi.org/10.1016/j.ijleo.2017.04.073

[16] Liu, H., Hua, G., Yin, H., & Xu, Y. (2018). An Intelligent Grey Wolf Optimizer Algorithm for Distributed Compressed Sensing. *Computational Intelligence and Neuroscience*, *2018*, 1-10. https://doi.org/10.1155/2018/1723191

[17] Luo, J., Chen, H., Wang, K., Tong, C., Li, J., & Cai, Z. (2017). LGWO: An Improved Grey Wolf Optimization for Function Optimization. *Lecture Notes in Computer Science*, *10385*, 99-105. https://doi.org/10.1007/978-3-319-59060-8_12

[18] Zha, Z., Zhang, X., Wang, Q., Tang, L., & Liu, X. (2018). Group-based sparse representation for image compressive sensing reconstruction with non-convex regularization. *Neurocomputing*, *296*, 55-63. https://doi.org/10.1016/j.neucom.2018.02.045

[19] Vinoth Kumar, K., Karthikeyan, S., Bhavani Sridharan, B., & Vennila Chockalingam, V. (2022). Performance improvement of SIMD processor for high-speed end devices in IoT operation based on reversible logic with hybrid adder configuration. *Tehnički vjesnik*, *29*(1), 252-258.

https://doi.org/10.17559/TV-20210719025814
[20] Polyakov, O., (2021). Development and research of a theoretical model of the magnetic tunnel junction. *Sensors*, *21*(6), 2118.
[21] Mohd Noor Sam, M. A. I., Jin, Z., Oogane, M., & Ando, Y. (2019). Investigation of a magnetic tunnel junction-based sensor for the detection of defects in reinforced concrete at high lift-off. *Sensors*, *19*(18), 4718. https://doi.org/10.3390/s19184718
[22] Fujiwara, K., (2018). Magnetocardiography and magnetoencephalography measurements at room temperature using tunnel magneto-resistance sensors. *Applied Physics Express*. https://doi.org/10.7567/APEX.11.023001
[23] Selvaraj, R., Pittala, S. S., & Duvvuri, E. C. (2024). Ct and MRI image reconstruction based single-path delay feedback (sdf) fft pipeline architecture. *Hellinic Journal of radiology*, *9*(2), 1-4.
[24] Kim, B., Lee, G. Y., & Park, S. H. (2023). Attention fusion network with self-supervised learning for staging of osteonecrosis of the femoral head (ONFH) using multiple MR protocols. *Medical Physics*, *50*(9), 5528-5540. https://doi.org/10.1002/mp.16380
[25] Fan, Y., Liao, H., Huang, S., Luo, Y., Fu, H., & Qi, H. (2024). A survey of emerging applications of diffusion probabilistic models in MRI. *Meta-Radiology*, *100*, 100082. https://doi.org/10.1016/j.metrad.2024.100082
[26] Murray, V., Siddiq, S., Crane, C., El Homsi, M., Kim, T. H., Wu, C. (2024). Movienet: Deep space-time-coil reconstruction network without k-space data consistency for fast motion-resolved 4D MRI. *Magnetic Resonance in Medicine*, *91*(2), 600-614. https://doi.org/10.1002/mrm.29892
[27] Kim, S., Park, H., & Park, S. H. (2024). A review of deep learning-based reconstruction methods for accelerated MRI using spatiotemporal and multi-contrast redundancies. *Biomedical Engineering Letters*, *14*, 1221-1242. https://doi.org/10.1007/s13534-024-00425-9

Contact information:

Nirmala R
Department of ECE,
Vivekanandha College of Engineering for Women (Autonomous),
Tiruchengode, Tamil Nadu, India
E-mail: drnirmalaece@gmail.com

Senthilkumar V M
Department of Electronics Engineering (VLSI Design and Technology),
Rajalakshmi Institute of Technology (Autonomous),
Chennai - 600124, Tamil Nadu, India
E-mail: vm.senthilkumar.phd@gmail.com

Malathi M
Department of ECE, E.G.S. Pillay Engineering College,
Nagapattinam, Tamil Nadu, India
E-mail: malathi@egspec.org

Vinoth Kumar K
(Corresponding Author)
Department of CSE (AI & ML), SSM Institute of Engineering and Technology,
Dindigul, Tamil Nadu, India
E-mail: vinodkumaran87@gmail.com