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Cascaded Multi-Level Inverter with Asymmetrical Voltage Sources Using Multicarrier PWM Strategies

MURUGANANDHAM N.*, SURESH PADMANABHAN T.

Abstract: Advanced multilevel inverters are pivotal in modern power electronics for achieving low-distortion waveforms and minimizing voltage stress on switching elements. This study introduces a cascaded H-bridge inverter design that employs asymmetrical DC sources configured in a trinary sequence, successfully delivering higher output voltage levels with fewer components than conventional topologies. A multi-carrier PWM approach is implemented with three modulation schemes Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) which are systematically evaluated through both MATLAB/Simulink simulations and hardware tests using a dSPACE DS1103 controller. Key performance measures, including total harmonic distortion, RMS voltage, crest factor, and form factor, are rigorously assessed. Experimental findings confirm that the APOD strategy offers superior harmonic suppression, while the trapezoidal MCPWM method enhances waveform quality and alleviates switch voltage stress. The results validate the proposed topology as an efficient, scalable solution for advanced power conversion applications.

Keywords: asymmetric inverter; cascaded H-bridge topology; dSPACE; multi-carrier PWM; symmetrical; THD

1 INTRODUCTION

Multilevel inverters (MLIs) have gained significant importance in modern power electronics due to their capability to handle medium- and high-power applications such as electric drives, HVDC transmission, and renewable energy integration [1]. Their ability to generate high-quality output waveforms with reduced voltage stress on switches and minimized electromagnetic interference has made them a preferred choice in both industrial and research domains. Compared to traditional two-level inverters, MLIs offer improved efficiency, reduced harmonic distortion, and enhanced scalability, making them suitable for a broad spectrum of applications [2]. Several MLI topologies exist, including diode-clamped, flying capacitor, and cascaded H-bridge (CHB) structures, with the CHB configuration being one of the most widely adopted. CHB inverters are particularly valued for their modularity and flexibility [3]. However, conventional CHB designs often require multiple isolated DC sources for each H-bridge cell, which increases system complexity and cost. This requirement becomes more challenging as the number of voltage levels increases. To overcome these challenges, recent developments have focused on asymmetrical multilevel inverter designs, where cells are powered by unequal DC sources. Such asymmetrical configurations allow the generation of a greater number of voltage levels with fewer switches and DC sources, leading to more compact, cost-effective, and efficient inverter systems suitable for renewable energy and industrial applications [3, 4].

Binary (1:2:4...) and trinary (1:3:9...) voltage progressions are two well-known methods in the literature. Previous research has shown that these schemes can reduce components and create custom voltages, but most of them only look at simulation results, single modulation strategies, or do not do thorough experimental benchmarking [5]. Control techniques, especially pulse width modulation (PWM) strategies, are just as important as how the parts are put together when it comes to the quality and efficiency of the output. Compared to classical single-carrier PWM or more computationally intensive space vector approaches, multi-carrier PWM (MC-PWM) methods like phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) allow for better harmonic suppression and voltage use [6, 7]. Previous research often evaluates only one PWM method, provides limited hardware validation, or does not offer a comprehensive comparison that links control logic to physical performance in asymmetrical topologies [8, 9]. Recent advancements in the field have developed asymmetrical MLI topologies and enhanced control algorithms; however, significant deficiencies persist:

- Model predictive and hybrid PWM techniques have shown great power quality and control flexibility, but they are not often tested on hardware for nine-level trinary systems.
- Research on binary-source reductions has led to significant increases in device count, but these often come at the expense of voltage flexibility, scalability, or dependence solely on simulation data.
- Numerous reviews and vehicle-centric studies enumerate MLI topologies; however, direct quantitative comparisons between modulation strategies and their effects on experimental THD, RMS voltage, and output waveforms are largely lacking.
- Most hardware prototypes are limited to symmetrical or lower-level (≤ 7) asymmetrical designs, which means that the experimental behaviour of higher-level, trinary AVSCMLIs is insufficiently explored.

This paper fills existing research gaps by proposing and experimentally validating an innovative nine-level Asymmetrical Voltage Source Cascaded Multilevel Inverter (AVSCMLI) topology. The main contributions and distinguishing features of this study include:

- Control Logic and Switching Methodology: Implementation of MC-PWM techniques customized for trinary voltage source progression, with control algorithms optimized for both simulation environments and real-time applications.
- Physical Hardware Realization and Experiments: The proposed inverter structure is developed using only two unequal DC sources and eight power switches, which minimizes hardware complexity and switching

requirements. The experimental validation is carried out on a dSPACE DS1103 platform, ensuring reliable digital interfacing and efficient implementation for practical testing.

- Extensive Comparative Evaluation: Presentation of both simulated and experimental data, offering detailed comparisons of harmonic distortion, waveform quality, voltage utilization, and complexity among prominent multicarrier PWM approaches over a range of modulation indices.
- In-depth Analytical Assessment: Provision of both quantitative and qualitative evaluations of voltage stress, harmonic spectra (using FFT and THD metrics), and form and crest factors, establishing clear correlations with modulation techniques and hardware performance.

By combining sophisticated control schemes, streamlined hardware design, and thorough benchmarking of modulation methods, this study delivers a consolidated and experimentally substantiated AVSCMLI framework exhibiting versatile voltage adaptability and enhanced power quality. To date, no prior studies have offered an equivalent comprehensive experimental and comparative analysis involving control strategies, switching optimizations, and detailed performance characterization for trinary-source nine-level cascaded multilevel inverters.

2 MULTILEVEL INVERTER

Multilevel inverters represent a major step forward in power electronics, as they are capable of producing high-quality output voltages by combining several DC sources. This architecture surpasses conventional two-level inverters by significantly reducing the harmonic distortion in output voltages, which minimizes the necessity for extensive filtering components and improves overall power quality. By spreading the total voltage across several switching devices, multilevel inverters reduce voltage stress, thereby enhancing device lifespan and system reliability [3, 10]. The most prevalent topology, the Cascaded H-bridge (CHB) inverter, offers two main configurations: symmetrical and asymmetrical. In symmetrical CHB designs, all H-bridge modules operate with equal DC inputs. Although this method is easier to design and control, it usually demands more modules to reach a given output voltage level. In contrast, the asymmetrical CHB arrangement assigns different DC voltage values to each H-bridge, typically based on binary or ternary progressions. This structure enables the generation of more voltage levels while using fewer modules, thereby enhancing efficiency and minimizing the number of components needed for comparable output quality. Recent studies indicate that when optimization techniques are applied, asymmetrical CHB systems achieve lower total harmonic distortion (THD) and offer greater flexibility for integration with renewable energy sources and intelligent grid networks [11, 12].

Control strategies have evolved rapidly, with techniques such as MC-PWM and nearest-level modulation enabling highly granular switching and dynamic harmonic suppression. These methods are central to current efforts to optimize inverter performance, particularly in solar photovoltaic, wind, and electric vehicle applications, where efficiency and power quality are paramount [13-15]. Recent developments, such as artificial intelligence, real-time optimization, and advanced modulation, have boosted the efficiency and adaptability of multilevel inverters, making them vital for renewable and high-power applications. Fig. 1 shows the block diagram of the AVSCMLI using MCPWM, where cascaded H-bridge cells are arranged in a modular fashion, and the total output is obtained by addition of the instantaneous voltages from each source in Eq. (1).

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + ... + v_{o,N}(t) \quad (1)$$

Here, N denotes the total number of cascaded H-bridge modules, and the overall inverter output voltage is, $v_o(t)$.

Symmetrical Cascaded Multilevel Inverter: In this topology, each H bridge cell is powered by an identical DC voltage source.

Asymmetrical Cascaded Multilevel Inverter: This configuration employs H-bridge modules with unequal DC voltage sources.

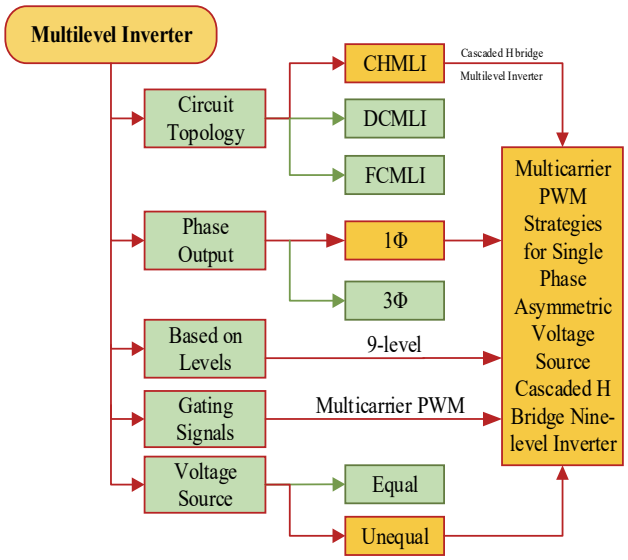


Figure 1 Proposed single phase asymmetric nine level inverter with MCPWM

2.1 Symmetrical Cascaded Multilevel Inverter

Cascaded H-bridge inverters are based on a modular structure, where multiple power conversion units are connected in series, each powered by its own isolated DC supply. Such an arrangement allows the production of a multi-step output voltage waveform [16]. A significant advantage of this topology lies in its modularity, which permits individual control and protection of each H-bridge cell. However, a key distinction from other multilevel inverter topologies, such as diode-clamped or flying capacitor designs, is the inherent requirement for multiple isolated DC power sources for each cell. While the CHB topology offers compelling benefits, including inherent modularity, the capacity to achieve high-voltage operation using lower-voltage devices, and strong suitability for integration with renewable energy sources, its implementation necessitates a higher component count and introduces increased control complexity due to the multiple

isolated DC sources [17]. Recent advancements have focused on enhancing the functionality of CHB converters, notably through the incorporation of voltage boosting capabilities within each H-bridge cell. This innovation facilitates single-stage power conversion, thereby further improving the topology's performance while preserving its fundamental modularity [18].

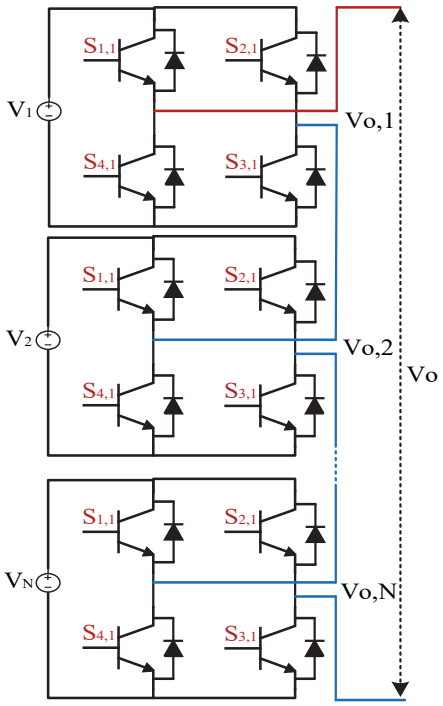


Figure 2 General structure of single phase symmetrical cascaded multilevel inverter

Fig. 2 depicts the typical layout of a symmetrical cascaded H-bridge multilevel inverter. The figure shows that the structure is made up of *n* series-connected bridges, each powered by an identical DC voltage source. For this symmetrical cascaded H-bridge inverter configuration, where all DC sources have the same voltage value ($V_{dc,1} = V_{dc,2} = \ldots = V_{dc,N} = V_{dc}$), the total possible number of output voltage steps and the maximum output voltage (v_o) are expressed by Eqs. (2) and (3) [19]:

$$L_{sym} = 2N + 1 \tag{2}$$

$$v_{o,max} = N \times v_{dc} \tag{3}$$

Here, N denotes the total number of cascaded H-bridge modules, L_{sym} denotes the level of symmetrical inverter.

2.2 Asymmetrical Cascaded Multilevel Inverter

Although symmetrical cascaded multilevel inverters have their benefits, asymmetrical versions are gaining traction because of several distinctive advantages:

Reduced number of components: Asymmetrical multilevel inverters can generate an equal number of voltage levels as their symmetrical counterparts while using a reduced number of DC power sources and switching devices. This reduction in components results in lower cost, smaller size and simplified control complexity [20].

Flexibility in selecting DC sources: Asymmetrical multilevel inverters provide enhanced adaptability by allowing the use of DC sources with varied voltage levels. This capability is especially advantageous in renewable energy systems, where power sources like solar panels and fuel cells often produce different output voltages [21].

Optimized Performance: Through strategic selection of the voltage ratios among DC sources, asymmetrical multilevel inverters can deliver enhanced performance, including reduced harmonic distortion and diminished switching losses, when compared to symmetrical designs [22].

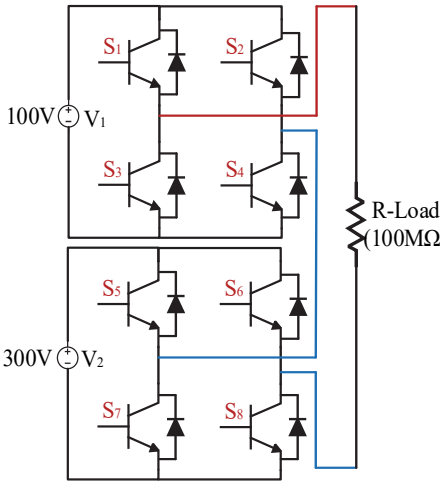


Figure 3 Proposed asymmetric voltage source cascaded nine level inverter

Cascaded H-bridge multilevel inverters use separate DC power sources for each H-bridge module to synthesize an AC voltage waveform. While symmetrical CMLIs use common DC sources for all H-bridges, the requirement for multiple sources increases complexity and cost, especially at higher voltage levels. Asymmetrical voltage source CMLIs overcome this limitation by using unequal DC sources. This asymmetry voltage distribution offers increased flexibility in regulating the output voltage and enables the generation of more voltage levels while using fewer components than symmetrical configurations. By strategically selecting DC voltage ratios, AVSCMLIs offer a more cost-effective and efficient approach to generating multi-level waveforms [19, 22].

An AVSCMLI with N H-bridges can produce many different output voltages, as described by the equation. Each H-bridge cell, with three possible switching states, contributes to the total output voltage by selectively adding or subtracting its corresponding DC voltage level. This combinatorial effect of the individual switching states of the H-bridge leads to a wide range of achievable output voltages. Two common AVSCMLI configurations use binary and trinary DC voltage sequences given in Eqs. (4) to (9). For N-H bridge inverters, a binary sequence follows a ratio of 1:2:4: ... :2N for DC voltage magnitudes, resulting in a maximum output voltage of $(2N - 1)V_{dc}$. Trinary sequences, on the other hand, use a ratio of 1:3:9: ... :3N, giving a maximum output voltage of $((3N - 1)/2)V_{dc}$ [21, 22] are given in Tab. 1.

Binary Progression:

$$v_{dc,j} = 2^{j-1} V_{dc} \left(j = 1,2,...,N\right) \tag{4}$$

and the maximum level is:

$$L_{bin} = 2^{N+1} - 1 \tag{5}$$

where, L_{bin} is binary Level of the inverter with maximum output voltage:

$$V_{o,max}^{bin} = \left(2^{N} - 1\right) V_{dc} \tag{6}$$

Trinary Progression:

$$v_{dc,j} = 3^{j-1} V_{dc} \left(j = 1,2,...,N\right) \tag{7}$$

total possible output levels:

$$L_{tri} = 3^{N} \tag{8}$$

where, L_{tri} is trinary Level of the inverter with maximum output voltage:

$$V_{o,max}^{tri} = \left(\frac{3^{N} - 1}{2}\right) V_{dc} \tag{9}$$

For the nine-level inverter example (trinary, two sources $V_1 = V_{dc}$, $V_2 = 3V_{dc}$):

$$V_o \in \{-4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}\} \tag{10}$$

When two DC voltage sources V_1 and V_2 are available, the possible voltage combinations include:

1. Single-level voltages: V_1, V_2, $-V_1$ and $-V_2$
2. Two-level combinations: $(V_1 + V_2)$, $-(V_1 + V_2)$, $(V_1 - V_2)$ and $(V_2 - V_1)$
3. Zero level: one

Table 1 Comparison of multilevel inverter

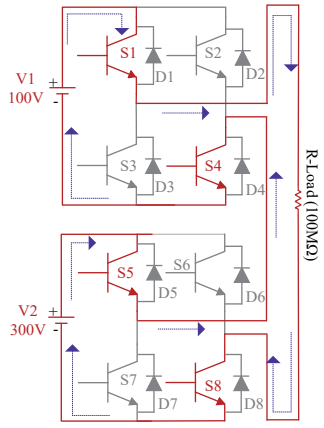
Topology Type	Symmetrical	Asymmetrical (Binary)	Asymmetrical (Trinary)
Voltage Sequencing[a]	Equal (V_{dc})	1:2:4 ...	1:3:9 ...
Number of Output Levels[b]	$2N + 1$	$2^{N+1} - 1$	3^N
Number of DC Sources	N	N	N
Number of Switches	$4N$	$4N$	$4N$
$V_{o\,Max}$)[c]	$N\,V_{dc}$	$2^N - 1\,V_{dc}$	$(3^N - 1)/2\,V_{dc}$

[a]Voltage Sequencing: Configuration of DC source magnitudes in each cell. [b]Number of output Levels: The distinct states (steps) generated at the output; e.g., for N cells, symmetrical yields $2N + 1$ levels. [c]Maximum output Voltage ($V_{o,max}$): The absolute peak phase voltage achievable by each topology for the given DC source arrangement.

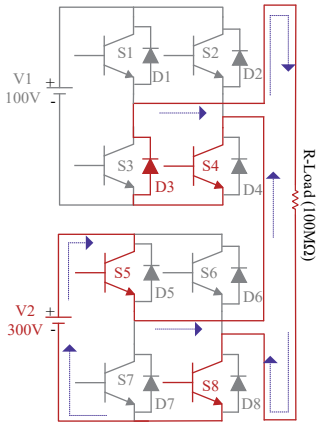
The proposed AVSCMLI can be achieved with just two asymmetrical DC voltage sources by carefully managing the switching configurations. The redundancy present in producing these voltage levels helps lower the total number of unique output states needed, which simplifies the design. As shown in Fig. 3, the proposed setup arranges the DC sources and switches to generate all possible voltage additions and subtractions. Furthermore, the detailed working details of the Asymmetrical Voltage Source Cascaded Multilevel Inverter (AVSCMLI) are presented in Tab. 2, highlighting the practical implementation of this approach and the Different switching states of the proposed Asymmetric Voltage Source Cascaded nine level inverter as shown in Fig. 4.

Table 2 Various switching states for nine-level inverter

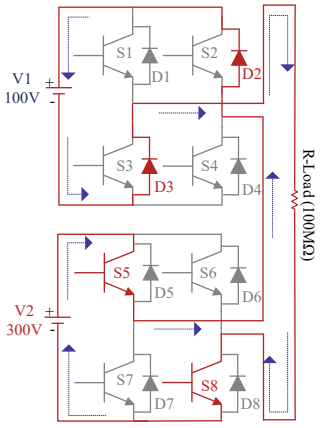
Mode	Load current path	Active Sources	Switching States (1 = ON , 0 = OFF)								Output
			S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	$V_1 - S_1 - S_8 - V_2 - S_5 - S_4 - V_1$	$V_1 + V_2$	1	0	0	1	1	0	0	1	$4V_{dc}$
2	$V_2 - S_5 - S_4 - S_3 - S_8 - V_2$	V_2	0	0	1	1	1	0	0	1	$3V_{dc}$
3	$V_2 - S_5 - S_2 - V_1 - S_3 - S_8 - V_2$	$V_2 - V_1$	0	1	1	0	1	0	0	1	$2V_{dc}$
4	$V_1 - S_1 - S_8 - S_7 - S_4 - V_1$	V_1	1	0	0	1	0	0	1	1	V_{dc}
5	$V_1 - S_1 - S_8 - S_7 - S_2 - V_1$	0	1	1	0	0	1	1	0	0	0
6	$V_1 - S_3 - S_8 - S_7 - S_2 - V_1$	$-V_1$	0	1	1	0	0	0	1	1	$-V_{dc}$
7	$V_1 - S_1 - S_6 - V_2 - S_7 - S_4 - V_1$	$-V_2 + V_1$	1	0	0	1	0	1	1	0	$-2V_{dc}$
8	$V_2 - S_7 - S_2 - S_1 - S_6 - V_2$	$-V_2$	1	1	0	0	0	1	1	0	$-3V_{dc}$
9	$V_1 - S_3 - S_6 - V_2 - S_7 - S_2 - V_1$	$-V_1 - V_2$	0	1	1	0	0	1	1	0	$-4V_{dc}$



$4V_{dc}$ ($V_1 - S_1 - S_8 - V_2 - S_5 - S_4 - V_1$)



$3V_{dc}$ ($V_2 - S_5 - S_4 - S_3 - S_8 - V_2$)



$2V_{dc}$ ($V_2 - S_5 - S_2 - V_1 - S_3 - S_8 - V_2$)

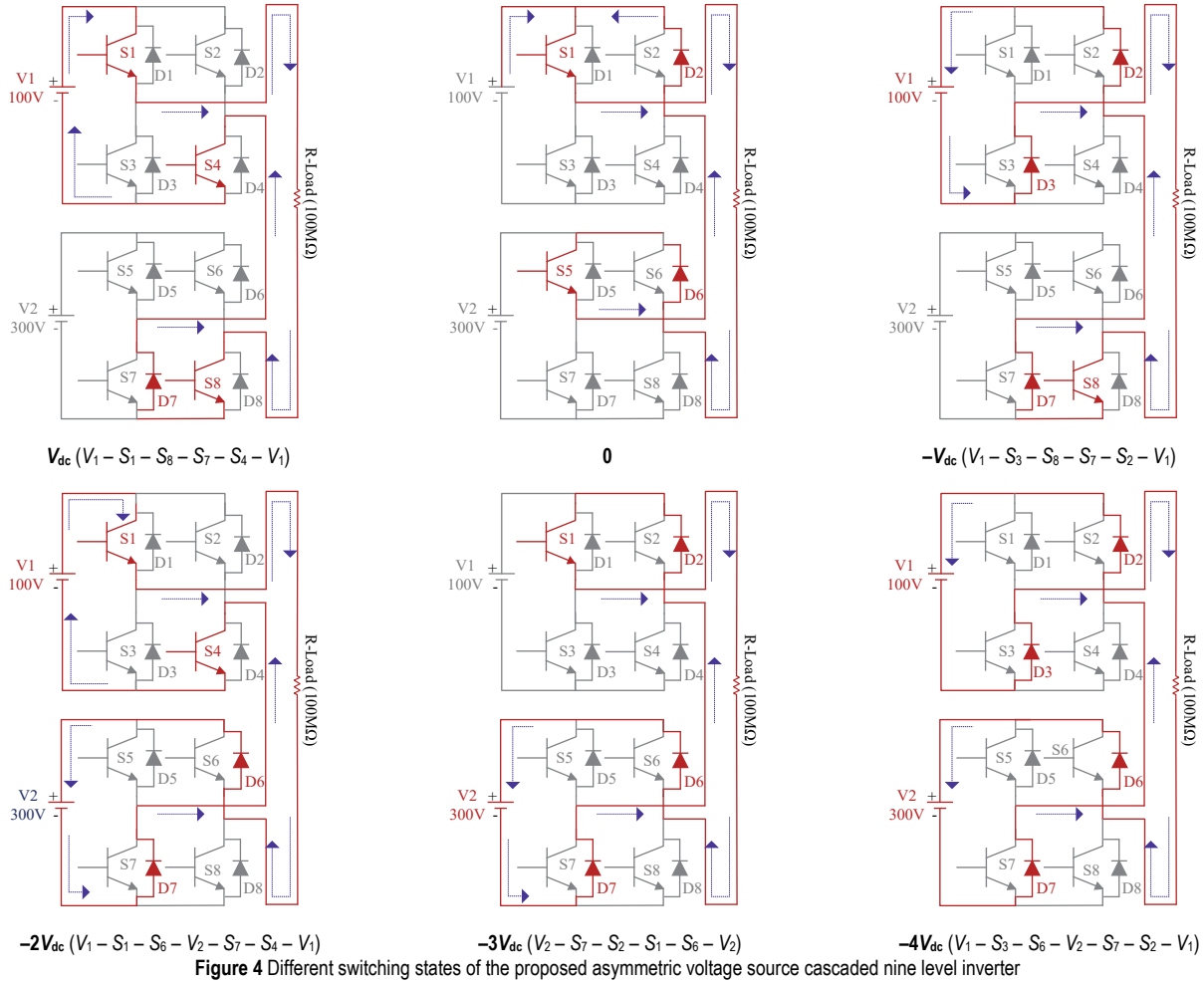


Figure 4 Different switching states of the proposed asymmetric voltage source cascaded nine level inverter

3 MODULATION SCHEME FOR MULTILEVEL INVERTERS

Modulation methods are crucial for managing the output voltage in multilevel inverters. These techniques dictate how the semiconductor switches operate, enabling accurate control over important waveform characteristics such as frequency, amplitude, and harmonic content. By carefully controlling the switching sequences, modulation schemes help to generate output voltages that meet the performance and quality standards. Careful selection of an appropriate modulation strategy is of utmost importance for optimizing inverter performance metrics, including minimizing harmonic distortions and maximizing efficiency [23]. The scheme of the various PWM techniques is shown in Fig. 5.

3.1 Categories of Modulation Schemes

Modulation strategies for multilevel inverters can be broadly classified into three main types [24]:

Space vector modulation: SVM methods provide improved performance in terms of harmonic distortion and DC bus voltage utilization. These techniques represent inverter switching states as vectors within a complex plane and synthesize the desired output voltage vector through a combination of adjacent vectors. However, Space vector modulation is computationally intensive for higher-level inverters, making it less suitable for real-time embedded systems.

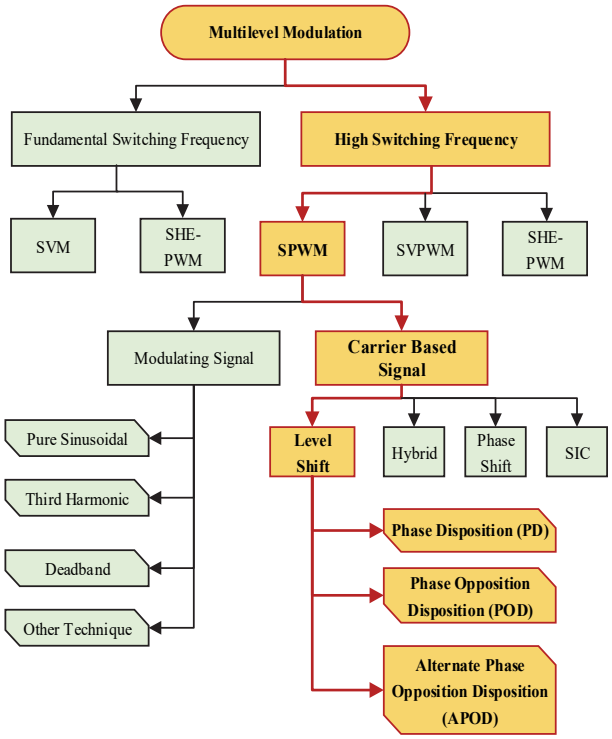


Figure 5 Details of PWM techniques

Carrier-based pulse width modulation: Carrier-based PWM techniques use multiple carrier signals to produce the switching pulses required by the inverter's power devices. Major CBPWM methods include phase-

shifted PWM (PS-PWM), level-shifted PWM (LS-PWM), and phase-disposition PWM (PD-PWM). In PS-PWM, several carrier waves have the same frequency and amplitude but are shifted in phase relative to each other. LS-PWM uses carriers with identical frequency but different voltage amplitude levels to generate switching signals. These approaches manage the inverter's switching devices to shape the output waveform effectively while controlling harmonic distortion and switching losses. PD-PWM combines aspects of PS-PWM and LS-PWM. Although generally easier to implement than SVM, carrier-based PWM methods can exhibit higher harmonic distortion, especially at lower switching frequencies.

Selective harmonic elimination: SHE techniques concentrate on removing particular harmonics from the output voltage waveform through the pre-calculation of optimal switching angles. This method allows precise control of harmonic content, but can be complex to implement, especially for inverters with numerous levels and different modulation indices. Selecting a suitable modulation scheme depends on various factors, including the number of levels of the inverter, the switching frequency and the specific application requirements.

While SVM provides good harmonic performance, it is computationally intensive, especially for high-level inverters. SHE offers precise harmonic elimination but lacks flexibility for real-time control. Carrier-based methods are widely used for their simplicity and adaptability, particularly for cascaded inverters [25].

4 MULTI-CARRIER PULSE WIDTH MODULATION

Multilevel inverters have been controlled using a variety of modulation techniques, such as space vector modulation and multicarrier pulse width modulation. Nevertheless, these techniques frequently employ high switching frequencies, which raises switching losses. By comparing carrier signals with a reference signal, multi-carrier PWM determines device switching. The resulting pulses regulate device switching based on predetermined voltage levels [26, 27]. With a focus on three alternative PWM strategies with various phase relationships, this section outlines the fundamentals of carrier-based PWM strategies for multilevel inverters.

- Phase Disposition (PD)
- Phase Opposition Disposition (POD)
- Alternative Phase Opposition Disposition (APOD).

4.1 Phase Disposition (PD)

A pulse width modulation method called phase disposition is used to regulate multilevel inverters' output voltage. Phase Disposition (PD) PWM is a widely used method for controlling multilevel inverters due to its simple implementation and good harmonic performance. While it provides moderate voltage utilization, its balance of ease and effectiveness makes it practical for high-power applications, particularly cascaded H-bridge inverters. [28]. PD uses multiple carrier signals with the same frequency and amplitude, each assigned to a specific cell or module within the multilevel inverter. However, unlike phase-shifted PWM, in which carriers are out of phase, in PD all carrier signals are in phase with each other as shown in Fig. 6 and the pulse waveforms corresponding to phase disposition scheme is shown in Fig. 7. During the modulation procedure, a sinusoidal reference waveform is compared with carrier signals. The points where the reference waveform intersects with the carrier signals define the switching instants for the respective inverter cells. It offers the advantages of a simplified control, good harmonic behavior and balanced voltage distribution. The limitations of PDPWM are voltage utilization, the output voltage amplitude may be slightly lower for a given DC bus voltage, and the switching frequency of individual devices in PD is relatively low, which could lead to higher filter requirements to achieve a very low THD.

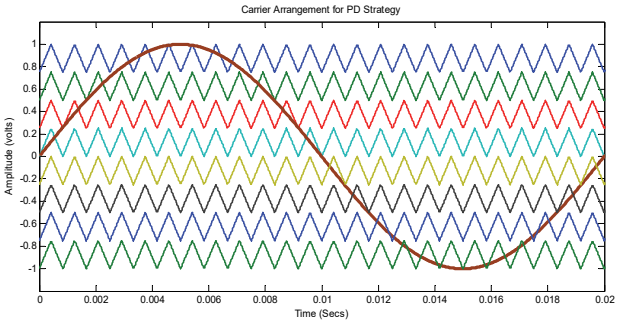


Figure 6 Carrier position for phase disposition

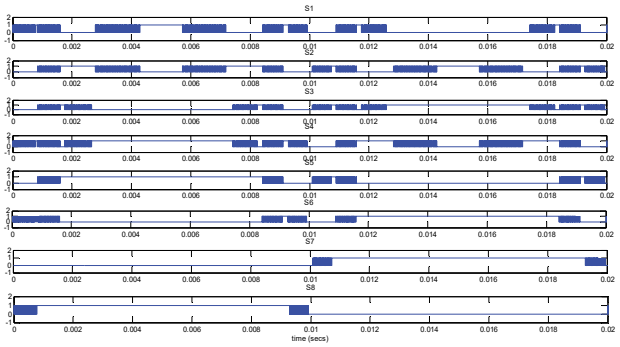


Figure 7 Waveforms corresponding to phase disposition modulation scheme

4.2 Phase Opposite Disposition (POD)

Phase Opposition Disposition (POD) pulse width modulation is a carrier-based technique used in multilevel inverters to generate switching signals for semiconductor devices. POD uses multiple triangular carrier signals, each associated with a specific inverter voltage level. These carrier signals have the same frequency and amplitude but are arranged in a specific phase relationship [28]. Phase Opposition Disposition (POD) PWM features carrier signals above and below the zero reference with a 180° phase difference as shown in Fig. 8 and and the pulse waveforms corresponding to phase opposition disposition scheme is shown in Fig. 9. This design helps reduce specific harmonics, resulting in lower distortion and balanced switching shown. While it is easy to implement and produces symmetrical device operation, POD offers less flexibility in harmonic shaping compared to selective harmonic elimination and may yield slightly lower output amplitude for the same DC voltage.

Phase Opposition Disposition is a valuable PWM technique for multilevel inverters that provides a balance between harmonic reduction, ease of implementation, and

symmetrical device switching. Its suitability for specific applications depends on factors such as desired harmonic performance, voltage utilization requirements, and complexity control considerations.

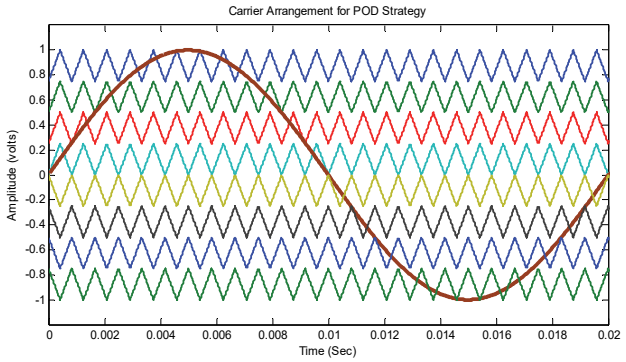


Figure 8 Carrier position for phase opposition disposition

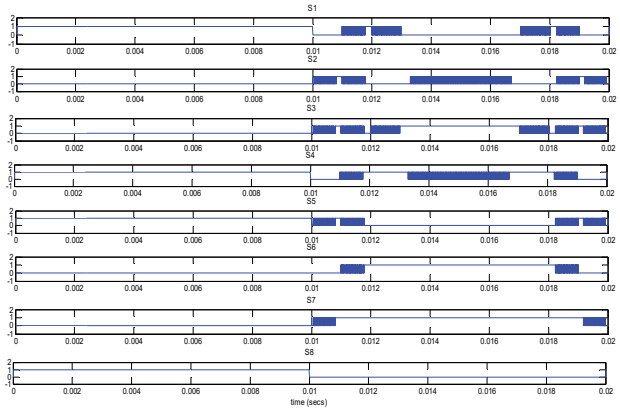


Figure 9 Waveforms corresponding to phase opposition disposition modulation scheme

4.3 Alternate Phase Opposite Disposition (APOD)

Alternative Phase Opposition Disposition (APOD) is a carrier-based PWM method used in multilevel inverters, similar to Phase Opposition Disposition (POD). In APOD, adjacent carrier signals are shifted by 180° relative to each other. This technique effectively reduces harmonic distortion in the output voltage and often results in better total harmonic distortion (THD) performance compared to POD, due to the cancellation of certain harmonic components in the line-to-line voltages [29]. However, instead of phase opposition based on the reference waveform, APOD arranges carrier signals in an alternating phase manner.

With APOD, each carrier signal is 180 degrees out of phase with its immediately adjacent carrier signals. This alternating phase pattern applies to all carrier signals, regardless of their position relative to the reference waveform. This arrangement produces a different harmonic cancellation pattern compared to the POD as shown in Fig. 10 and the pulse waveforms corresponding to alternative phase opposition disposition scheme is shown in Fig. 11.

Harmonic Content: While both APOD and POD reduce harmonic distortion, they target different harmonic orders. The specific harmonic cancellation pattern of each method results in different THD values for a given number of levels and modulation index.

Voltage Utilization: APOD typically results in slightly lower voltage utilization compared to POD. It offers a good compromise between harmonic reduction and ease of implementation in multilevel inverters. The choice between APOD and POD depends on application-specific needs, including harmonic performance and voltage utilization considerations.

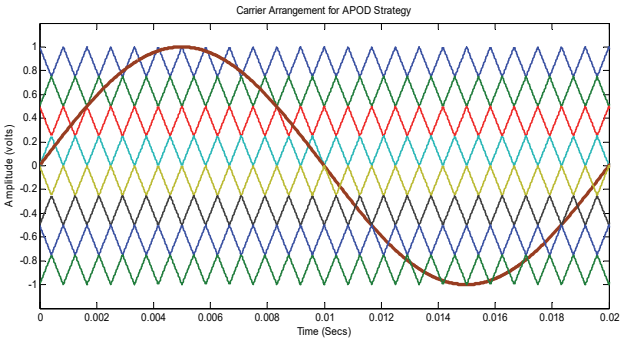


Figure 10 Carrier position for alternative phase opposition disposition

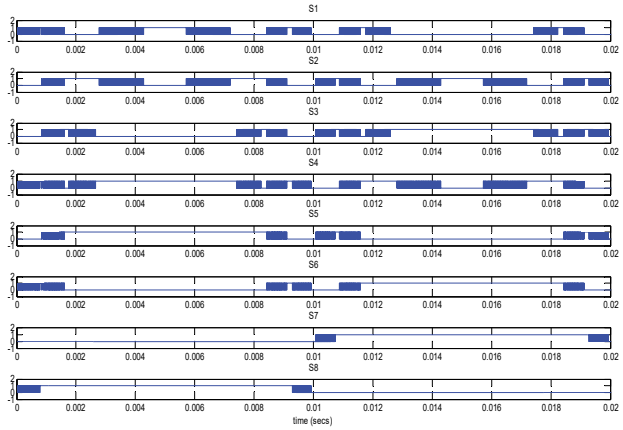


Figure 11 Waveforms corresponding to phase opposition disposition modulation scheme

5 SIMULATION RESULTS

Asymmetrical multilevel inverters represent a compelling alternative to their symmetrical counterparts, offering higher voltage capabilities with a reduced component count. However, the inherent asymmetry of DC voltage sources leads to complexity in control strategies. Multicarrier pulse width modulation techniques provide an effective solution for AVSCMLI control, enabling flexible and efficient operation. This research examines the synergy between AVSCMLIs and MC-PWM and examines their underlying principles, advantages, challenges, and potential applications. Simulation studies conducted in MATLAB/Simulink validate the proposed multi-carrier PWM strategies for a nine-level single-phase asymmetric cascaded H-bridge multilevel inverter, as shown below. The Simulink diagram of AVSCMLI with MCPWM as shown in Fig. 12.

Simulations were conducted over a modulation index range from 0.8 to 1.0 to evaluate the performance of the inverter. The THD of the output voltage was assessed using a Fast Fourier Transform (FFT) block, which analysed the harmonic content. Additionally, the RMS value of the fundamental component of the output voltage was recorded to quantify voltage magnitude. These simulation results

provide insight into the harmonic performance and voltage quality under various modulation conditions. The following simulation parameters were used: $V_1 = 100V_{dc}$, $V_2 = 300V_{dc}$, $f_c = 1200$ Hz and $R_{load} = 100$ MΩ.

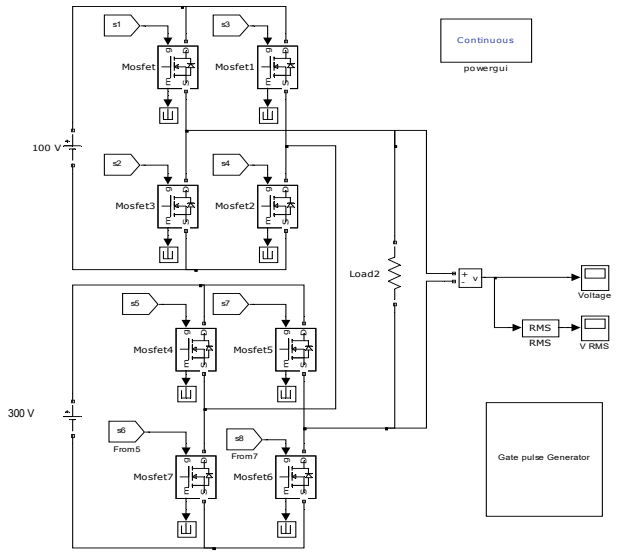


Figure 12 Simulink diagram of asymmetric voltage source cascaded nine level inverter with MCPWM

The simulated output voltage waveform using Phase Disposition PWM shows a clear nine-level stepped structure with good symmetry around zero as shown in Fig. 13. The FFT spectrum (Fig. 14) indicates dominant lower-order harmonics around the 9th and 11th orders, with a calculated THD of 4.22%. Although THD is slightly higher compared to POD and APOD, the waveform remains stable and distortion is minimized at unity modulation index.

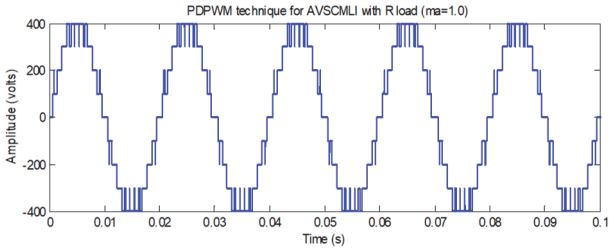


Figure 13 Simulated output voltage produced by PDPWM technique for *R* load with $m_a = 1.0$

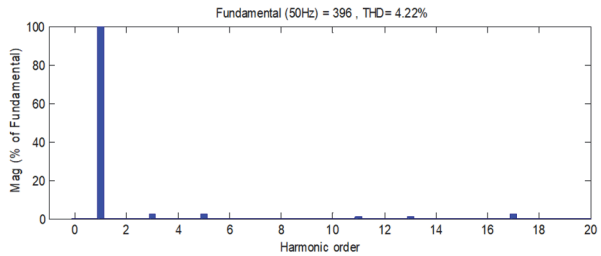


Figure 14 FFT analysis produced by PDPWM strategy with $m_a = 1.0$

The POD strategy produces a similar nine-level output but with noticeably smoother staircase transitions, as evident in Fig. 15. The FFT spectrum in Fig. 16 shows lower harmonic magnitudes in the 11th-15th range compared to PD. As a result, the THD reduces to 3.42%. This confirms the effectiveness of POD in suppressing certain symmetrical harmonics, consistent with literature.

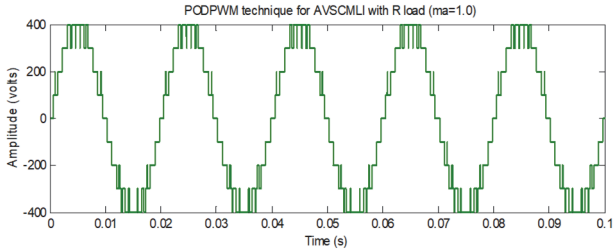


Figure 15 Simulated output voltage produced by POD technique for *R* load with $m_a = 1.0$

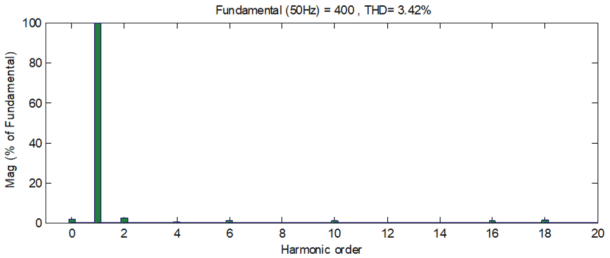


Figure 16 FFT analysis produced by PODPWM strategy with $m_a = 1.0$

The APOD waveform is nearly identical in appearance to POD, but its harmonic spectrum (Fig. 17) reveals different cancellation patterns. The FFT shows suppressed even harmonics but slightly higher peak content around the 17th and 19th orders as shown in Fig. 18. The THD is 3.46%, marginally higher than POD but comparable. Interestingly, at reduced modulation indices ($m_a = 0.9$ and 0.85), APOD's THD rises faster than POD (Tab. 3) a trade off between harmonic suppression and voltage utilization.

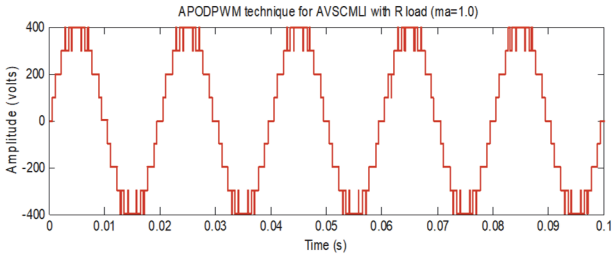


Figure 17 Simulated output voltage generated by APOD technique for R load with $m_a = 1.0$

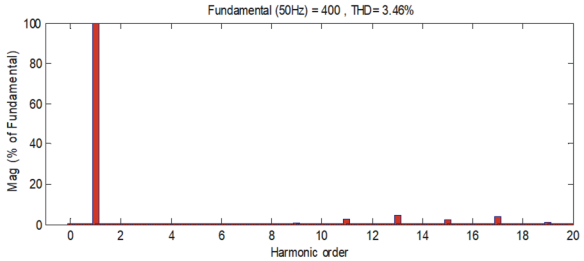


Figure 18 FFT analysis produced by APODPWM strategy with $m_a = 1.0$

In simulation, POD consistently gives the lowest THD, APOD is close, and PD is different. The harmonic spectrum clearly indicates that sharing phase opposition between upper and lower carriers is the reason for improved cancellation in POD.

Table 3 THD calculation for various MCPWM method

Modulation Index (MI)	Total Harmonics Distortion (%THD)		
	PD	POD	APOD
1.0	4.22	3.42	3.46
0.95	4.41	3.92	3.5
0.90	4.55	3.96	3.82
0.85	4.52	4.06	4.24
0.80	4.77	4.21	4.5

Table 4 V_{rms} (fundamental) of output voltage for different m_a

m_a	PD	POD	APOD
1	280	282.8	282.8
0.95	268.4	268.7	268.7
0.9	254	254.6	254.5
0.85	240.3	240.4	240.4
0.8	227.6	226.3	226.2

Table 5 Crest factor (CF) of output voltage for different m_a

m_a	PD	POD	APOD
1	1.414	1.414	1.414
0.95	1.414	1.414	1.414
0.9	1.414	1.414	1.414
0.85	1.414	1.414	1.414
0.8	1.414	1.414	1.414

Table 6 Form factor (FF) of output voltage for different m_a

m_a	PD	POD	APOD
1	1.11	1.11	1.1098
0.95	1.11	1.11	1.11
0.9	1.1098	1.1097	1.1098
0.85	1.1098	1.11	1.11
0.8	1.11	1.11	1.11

Tabs. 4 to 6 compare PD, POD, and APOD strategies for the nine-level inverter. Results show that V_{rms} decreases with lower m_a, while Crest Factor (1.414) and Form Factor (1.11) remain nearly constant. Overall, all three strategies provide consistent voltage regulation and waveform quality, confirming the robustness of carrier-based PWM control.

6 EXPERIMENTAL RESULTS

This section examines modulation techniques that are particularly suitable for real-time implementation in asymmetrically cascaded multilevel inverters. The proposed AVSCMLI topology was implemented and tested using a dSPACE DS1103 controller board. The control logic was developed in MATLAB/Simulink and deployed in real time. Switching signals were generated through the 8-channel DAC interface of the DS1103 board and used to drive the gates of MOSFET switches via opto-isolated gate drivers. The resulting nine-level output voltages are presented and analyzed along with the corresponding percentages of THD, fundamental RMS voltage, form and crest factor values. Based on the DS1103 controller board, the dSPACE system is a stand-alone platform that integrates data collection and autonomous processing capabilities for the implementation of digital control. The DS1103 board, which is well-known for its adaptability in rapid prototyping, can be mounted in a PC or dSPACE expansion box, which facilitates control function testing in the lab. Its computing power and high-speed input/output capabilities are critical for applications involving multiple actuators and sensors.

6.1 dSPACE-Based PWM Strategy Implementation

Simulink was used to perform preliminary offline simulations of the gate signal generation blocks/models for the chosen nine-level inverter utilizing different PWM techniques. Following development, the Simulink models were downloaded, compiled, and executed in real time on a dSPACE system. Using the seamless Simulink-dSPACE interface, the "Build" function in Simulink automatically generated targeted C code via the dSPACE real-time workshop. This C code served as the source for the dSPACE real-time interface, which used a C compiler/linker to generate the machine code and download it to the dSPACE board. Finally, the dSPACE ControlDesk software provided a user-friendly graphical user interface for reading and writing internal control system variables, enabling observation of critical system data. External voltages in the range of –10 V to +10 V were quantized to –1 V to +1 V for the analog-to-digital conversion and vice versa for the digital-to-analog conversion unit of the dSPACE system. Gains of 0.1 and 10 were added to account for this signal conversion. Prior to being applied to the MOSFET gates of the prototype inverters, the generated switching pulses that were received from the DAC or the input/output ports of the dSPACE system were amplified. Fig. 19 shows the interface between the nine-level inverter and the dSPACE-based PWM switching signal generator.

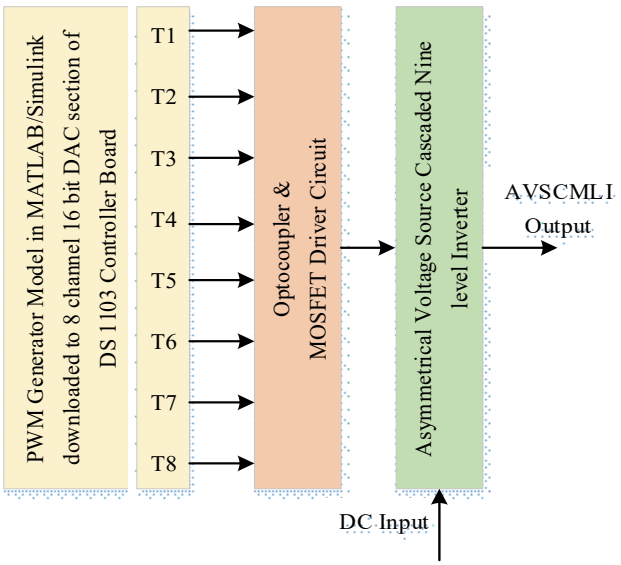


Figure 19 Block diagram of interfacing of nine-level inverter with dSPACE

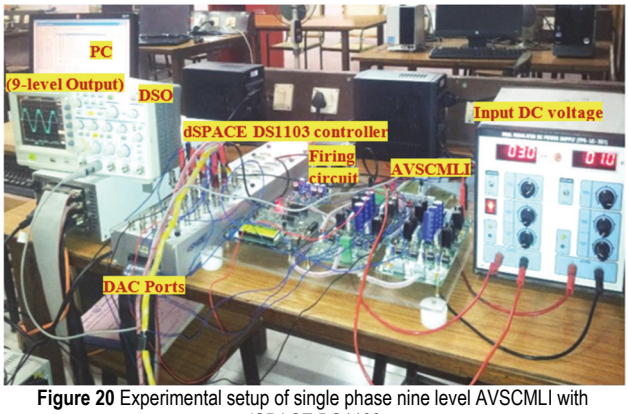


Figure 20 Experimental setup of single phase nine level AVSCMLI with dSPACE DS1103

The experimental setup for the proposed AVSCMLI is depicted in Fig. 20. The proposed studies validate the use of multicarrier-based PWM strategies for a chosen asymmetrical cascaded multilevel inverter. They are carried out with MATLAB/Simulink and dSPACE. The modulation index (m_a) range that was used to evaluate performance was 0.8 to 1.0. Power quality indices including V_{rms}, FF, CF and THD were experimentally evaluated and analyzed for the selected nine-level trinary voltage source cascaded multilevel inverter. The following hardware parameters were used: V_{dc} = 1 V and 3 V, f_c = 1200 Hz and R_{load} = 100 Ω.

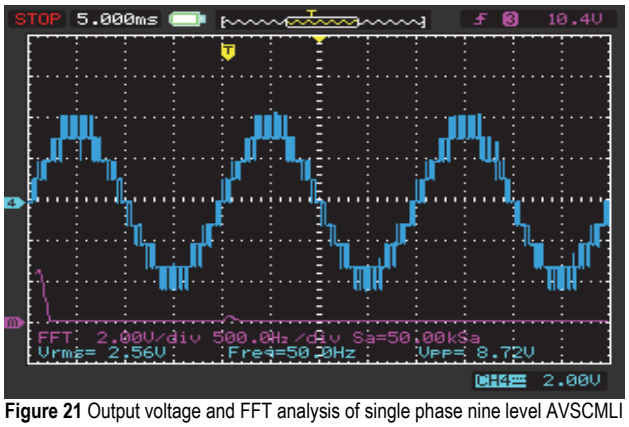


Figure 21 Output voltage and FFT analysis of single phase nine level AVSCMLI with PD technique for *R* load (m_a = 0.8)

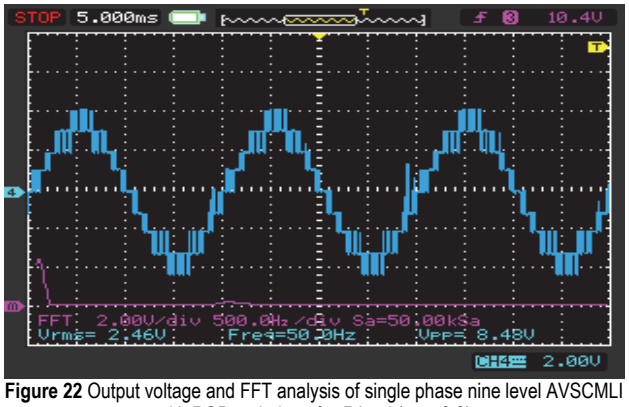


Figure 22 Output voltage and FFT analysis of single phase nine level AVSCMLI with POD technique for *R* load (m_a = 0.8)

The experimental results presented in Figs. 21 to 23 and Tab. 7 demonstrate the performance of the single-phase asymmetrical voltage source cascaded multilevel inverter (AVSCMLI) using Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) modulation strategies. At a modulation index of m_a = 0.8, the inverter produces a nine-level output waveform with good sinusoidal quality, while the FFT spectra confirm that lower-order harmonics are effectively suppressed, leaving only higher-order components. The corresponding THD values indicate that APOD achieves the best harmonic performance (4.82%) compared to POD (6.73%) and PD (8.72%), and this trend continues across all modulation indices. As ma increases from 0.8 to 1.0, THD decreases consistently, with APOD maintaining the lowest distortion levels (4.06% at m_a = 1.0), followed by POD (5.38%) and PD (6.98%). These results confirm that while all three carrier-based PWM techniques are effective for AVSCMLI operation, the APOD method offers superior waveform quality and reduced harmonic content, making it the most efficient choice for applications requiring improved power quality.

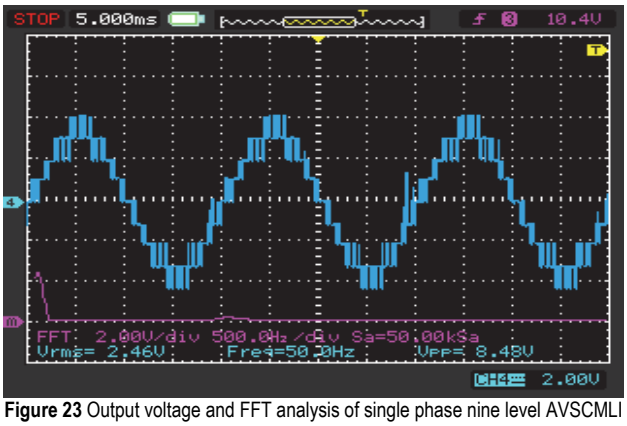


Figure 23 Output voltage and FFT analysis of single phase nine level AVSCMLI with APOD technique for *R* load (m_a = 0.8)

Table 7 %THD calculation of AVSCMLI various MCPWM method

m_a	PD	POD	APOD
1	6.98	5.38	4.06
0.95	7.34	5.67	4.26
0.9	7.75	5.98	4.28
0.85	8.21	6.33	4.54
0.8	8.72	6.73	4.82

Table 8 V_{rms} calculation of AVSCMLI various MCPWM method

m_a	PD	POD	APOD
1	3.55	3.68	3.67
0.95	3.39	3.57	3.56
0.9	3.3	3.5	3.45
0.85	3.08	3.38	3.37
0.8	2.56	2.46	3.36

Table 9 Crest factor calculation of AVSCMLI various MCPWM method

m_a	PD	POD	APOD
1	1.414	1.414	1.414
0.95	1.414	1.414	1.414
0.9	1.414	1.414	1.414
0.85	1.414	1.414	1.414
0.8	1.414	1.414	1.414

Table 10 Form factor calculation of AVSCMLI various MCPWM method

m_a	PD	POD	APOD
1	1.11	1.11	1.1098
0.95	1.11	1.11	1.11
0.9	1.1098	1.1097	1.1098
0.85	1.1098	1.11	1.11
0.8	1.11	1.11	1.11

The results presented in Tabs. 8 to 10 highlight the performance of the AVSCMLI under different modulation indices and PWM strategies. Table 8 shows that the RMS output voltage (Vrms) decreases as the modulation index (ma) reduces, with POD and APOD maintaining slightly better regulation compared to PD. Tab. 9 confirms that the Crest Factor (CF) remains constant at 1.414 for all cases, indicating a stable ratio of peak to RMS voltage. Meanwhile, Tab. 10 demonstrates that the Form Factor (FF) stays close to 1.11 with only negligible variation, ensuring consistent waveform quality. Overall, the results prove that all PWM methods deliver stable performance, while APOD achieves the best balance in terms of RMS output, voltage quality, and reduced THD.

Fig. 24 clearly compares the Total Harmonic Distortion (%THD) results obtained from simulation and

experimental methods for three MCPWM techniques: PD, POD, and APOD.

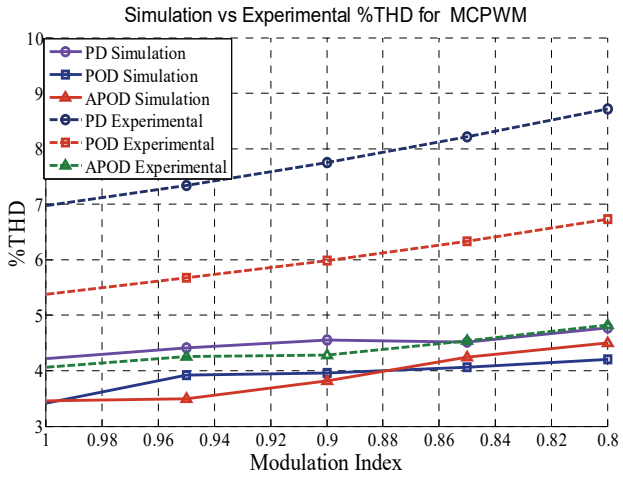


Figure 24 %THD comparison of simulation and experimental analysis for various modulation index

The experimental total harmonic distortion (%THD) values are consistently higher than the simulated values across all modulation indices. Among the modulation methods, Phase Disposition (PD) exhibits the highest %THD, followed by Phase Opposition Disposition (POD), while Alternate Phase Opposition Disposition (APOD) achieves the lowest %THD in both simulations and experimental results. This demonstrates the superior effectiveness of the APOD technique in minimizing harmonic distortion. Additionally, the data show that %THD tends to increase as the modulation index decreases, indicating reduced harmonic performance at lower modulation levels.

7 CONCLUSION

This study proposes and validates a nine-level Asymmetrical Voltage Source Cascaded Multilevel Inverter (AVSCMLI) that employs multicarrier PWM strategies tailored for trinary DC source configurations. The research builds a solid technical framework by integrating precise mathematical modeling, dimensioned circuit diagrams, and extensive simulation studies, further supported by real-time experimental validation using a dSPACE DS1103 platform. A detailed comparison of multi-carrier PWM modulation strategies highlights key trade-offs. PD-PWM ensures ease of implementation and balanced voltage sharing with satisfactory harmonic suppression. POD-PWM provides improved voltage utilization and stronger harmonic elimination. APOD-PWM provides a practical compromise by reducing harmonic distortion while maintaining moderate control complexity, although it results in slightly lower voltage utilization.

Simulation and hardware results across varying modulation indices confirm the ability of the proposed topology to generate high-quality output waveforms with fewer components, making it suitable for renewable energy integration and industrial applications. The findings reinforce the necessity of selecting PWM schemes based on application-specific requirements, balancing harmonic performance, voltage utilization, hardware simplicity, and cost-effectiveness.

Future research can extend this work by optimizing control algorithms and exploring modified topologies to further enhance performance, scalability, and adaptability. Overall, the presented analysis provides comprehensive insights and practical recommendations for advancing multilevel inverter technologies.

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Contact information:

MURUGANANDHAM N., Research Scholar
(Corresponding author)
Anna University, Chennai,
E. G. S. Pillay Engineering College (Autonomous), Nagapattinam,
Tamil Nadu, India
E-mail: nveeramurugan@gmail.com

SURESH PADMANABHAN T., Professor
Department of Electrical and Electronics Engineering,
E. G. S. Pillay Engineering College (Autonomous), Nagapattinam,
Tamil Nadu, India
E-mail: Sureshsilver@gmail.com