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Individual Phase Current Control Algorithm for Load Unbalance Compensation in Grid-Connected Three-Level Inverters Operating in Islanding Mode

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***Summary* — Grid-connected inverters must maintain a stable power supply to critical loads during islanding operation when grid faults occur. Imbalanced loads make it difficult to sustain balanced three-phase voltages and can seriously impair sensitive three-phase equipment. This paper proposes an individual phase current control algorithm for load imbalance compensation in grid-connected three-level inverters operating in islanding mode. The method uses a dual-loop control architecture: a D–Q frame voltage controller handles overall voltage regulation, while an ABC frame current controller provides per-phase current management. A key innovation is feedforward compensation using real-time load current measurements, combined with a static switch that enables flexible switching between three-wire and four-wire configurations. When a power-based detection algorithm identifies significant load imbalance, the system automatically transitions to four-wire mode, where independent control of each phase current is possible without the zero-sum constraint. The voltage controller operates at a 5–6Hz bandwidth in the D–Q frame; the current controller operates at a 1kHz bandwidth in the ABC frame for fast per-phase tracking. Simulation results show accurate current tracking—a 1.76A increase under a 100% load step and a 1.02A decrease under a 50% load reduction—while maintaining balanced voltages and reducing total harmonic distortion (THD) from 13.18% to 3.64%. The distinct novelty of this work lies in the tight integration of ABC-frame per-phase feedforward with automatic three-/four-wire reconfiguration, which avoids the coordinate-transformation overhead inherent in existing approaches and achieves a settling time two to three times faster than conventional D–Q-only methods.**

***Keywords* — Grid-connected inverter, individual phase current control, load imbalance compensation, three-level inverter, islanding mode, dual-loop control, feedforward compensation, static switch.**

I. Introduction

Grid-connected inverters are central to modern power systems, particularly for integrating renewable energy sources such as pho-tovoltaic and wind power systems.

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[1], [2]. These inverters operate in two distinct modes: grid-connected mode during normal conditions and standalone (islanding) mode when grid faults occur [3]. During islanding, the inverter must maintain power quality independently for critical loads that require uninterrupted operation [4].

The increasing penetration of distributed energy resources has intensified challenges in power quality and load management [5], [26]. Critical loads—hospitals, data centers, essential industrial processes—demand tightly regulated voltages with minimal frequency deviation [6]. Although these loads are predominantly designed for balanced three-phase conditions, the integration of singlephase loads and the inherent asymmetry in practical load distribution create significant voltage imbalance during islanding [7], [27].

Load imbalance is among the most significant challenges in islanding mode [8]. When the inverter supplies both critical three-phase loads and single-phase or imbalanced major loads, the resulting power asymmetry directly affects the three-phase voltage balance at the point of common coupling (PCC) [9]. Recent studies have shown that imbalanced grid conditions lead to double-line-frequency power oscillations, which worsen DC-link voltage ripple and stress DC-link capacitors [10], [28]. This voltage imbalance causes reduced efficiency, overheating, and potential equipment failure [11].

Conventional control strategies primarily rely on synchronous reference frame (d-q) methods, which assume balanced three-phase quantities [12], [13]. These approaches demonstrate significant limitations under imbalanced conditions, leading to steady-state errors and poor dynamic response [14], [15], [16]. Recent efforts include advanced low-voltage ride-through strategies [17], proportional-resonance controllers [18], and disturbanceobserver-based decoupled current approaches [19]. Fourleg voltage source inverters with space-vector hysteresis controllers have been applied in the αβ0 frame [20], and multi-functional grid-connected systems using αβc coordinates have been proposed for imbalanced loads [21].

State-feedback controllers using linear quadratic regulators have also been investigated [22]. More recently, model-predictive control [29], virtual synchronous machine strategies [30], and deep-learning-aided imbalance compensation [31] have been explored.

Despite these advances, existing solutions often suffer from complex coordinate transformations, poor performance under severe imbalance, or inability to control individual phase currents independently [23], [24], [25].

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Distinct Contribution of This Work

This paper proposes an individual phase current control (IPCC) algorithm that differs from existing approaches in three concrete ways.

1. **ABC-frame per-phase feedforward**: existing D– Q-only controllers generate current references in the synchronous frame and transform them to the natural frame; any per-phase load disturbance appears only after propagating through the voltage loop. The proposed algorithm injects the measured per-phase load current directly into the natural-frame current reference, providing instantaneous feedforward that the D–Q path cannot supply.
2. **Automatic three-/four-wire reconfiguration**: a power-deviation detection algorithm monitors perphase power in real time. When imbalance exceeds the threshold, a static switch closes to establish the neutral path, lifting the zero-sum constraint on phase currents without manual intervention or modeswitching transients. Returning to three-wire mode is equally automatic when balance is restored.
3. **Bandwidth-separated dual-loop architecture**: the outer voltage loop (5–6Hz bandwidth, D–Q frame) and the inner current loop (1kHz bandwidth, ABC frame) are designed with a 10–20× frequency separation, which provides stability guarantees absent in single-loop or same-bandwidth dual-loop designs.

Together, these features yield settling times two to three times shorter, current tracking errors below 2%, and THD compliant with IEEE 519, even under 100% single-phase load steps.

The remainder of this paper is organized as follows. Section II presents the system configuration and mathematical model. Section III describes the imbalance detection algorithm. Section IV details the proposed IPCC algorithm. Section V provides stability analysis and controller design. Section VI describes the simulation setup. Section VII presents and discusses simulation results. Section IX addresses practical implementation considerations. Section X concludes the paper.

II. System Configuration and Modeling

A. Grid-Connected Three-Level Inverter Configuration

The proposed system uses a three-level neutral-pointclamped (NPC) inverter connected to the utility grid through an L-C output filter. Compared with a two-level inverter, the three-level NPC topology offers lower harmonic distortion, reduced switching losses, and improved power quality [12]. The system operates in both gridconnected and islanding modes with seamless transition on grid fault detection.

The output filter comprises inductor L_f and capacitor C_f, chosen to attenuate voltage ripple while preserving dynamic performance. Critical loads (sensitive three-phase equipment) and major loads (single-phase or imbalanced three-phase loads) both connect at the PCC. The static switch enables reconfiguration between three-phase threewire and four-wire operation; it remains open underbalanced conditions and closes once significant imbalance is detected.

B. Load Configuration

Critical loads represent sensitive three-phase equipment—industrial motors, precision instruments, and critical infrastructure—that requires tightly regulated, balanced voltages. *Major loads* include single-phase or imbalanced three-phase loads that generate asymmetric power consumption and are the primary source of system imbalance. In three-wire mode the neutral is isolated, constraining the sum of phase currents to zero. In four-wire mode the static switch establishes a neutral path, allowing each phase current to be controlled independently.

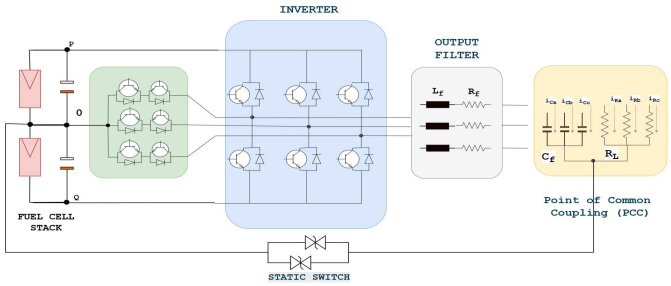

Fig. 1. Overall system configuration.

C. Mathematical Modeling

The three-level NPC inverter produces phase output voltages

$$v_{\mathrm{inv},abc} = S_{abc} \cdot \frac{V_{\mathrm{dc}}}{2}, \tag{1}$$

where $S \in \{-1,0,+1\}$ is the per-phase switching function and V_{dc} is the DC-link voltage. Equation (1) shows that the controller must synthesize the desired output voltage through the switching function; the maximum achievable phase voltage is $V_{dc}/2$.

The filter inductor dynamics that underlie the current control loop are

$$L_f \frac{\mathrm{d}i_{L,abc}}{\mathrm{d}t} = v_{\mathrm{inv},abc} - v_{C,abc}, \tag{2}$$

where $i_{L,abc}$ are the filter inductor currents (the quantities tracked by the inner loop) and $v_{C,abc}$ are the filter capacitor voltages (the quantities regulated by the outer loop). The capacitor node equation is

$$C_f \frac{\mathrm{d}v_{C,abc}}{\mathrm{d}t} = i_{L,abc} - i_{R,abc}, \tag{3}$$

where $i_{R,abc}$ are the per-phase load currents. Equation (3) reveals the load current as a disturbance input to the voltage loop; feedforward of $i_{R,abc}$ is the key mechanism that decouples load changes from voltage regulation.

D. Three-Wire versus Four-Wire Operation

In three-wire operation the instantaneous current constraint

$$i_{La} + i_{Lb} + i_{Lc} = 0 \tag{4}$$

prevents independent control of individual phase currents and limits the effective compensation of severe imbalance. When the static switch is closed, this constraint is lifted:

$$i_{La} + i_{Lb} + i_{Lc} = i_n \neq 0, \tag{5}$$

where i_n is the neutral current. The value of i_n quantifies the severity of imbalance and is monitored after switch closure to confirm four-wire operation. This transition is reflected in the control model by removing the constraint (4) and replacing it with (5), after which three independent current references i^*_{La}, i^*_{Lb}, i^*_{Lc} can be issued without any coupling.

E. System Parameters

Filter inductance L_f is chosen to limit current ripple to below 10% of rated current at the switching frequency, while preserving sufficient current-control bandwidth. Filter capacitance C_f is sized to provide reactive power support during load transients. The switching frequency balances switching losses against harmonic

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performance. DC-link voltage V_{dc} is set to maintain adequate modulation headroom across the required output voltage range. Numerical values are given in Table II.

III. Load Imbalance Detection and Analysis

A. Imbalance Metrics

Imbalance manifests as asymmetric power consumption, leading to unequal current magnitudes and phase displacements. Under four-wire operation, the neutral current i_n from (5) provides a direct measure of imbalance severity. Two standard metrics quantify imbalance. The current imbalance factor (CUF) is defined as

$$\mathrm{CUF} = \frac{\max\left(|I_a - I_{\mathrm{avg}}|,\ |I_b - I_{\mathrm{avg}}|,\ |I_c - I_{\mathrm{avg}}|\right)}{I_{\mathrm{avg}}} \times 100\%, \tag{6}$$

where $I_{\mathrm{avg}} = (I_a + I_b + I_c)/3$ and I_a, I_b, I_c are the RMS phase currents. The voltage imbalance factor (VUF) is

$$\mathrm{VUF} = \frac{V^-}{V^+} \times 100\%, \tag{7}$$

where V^- and V^+ are the negative- and positive-sequence RMS voltages, respectively. Threshold values for CUF and VUF, together with the power-deviation criterion below, trigger the four-wire control mode.

B. Power-Based Detection Algorithm

Per-phase instantaneous power provides better sensitivity to imbalance than current-only or voltage-only approaches because it captures both magnitude and phase distortions simultaneously. Per-phase power is computed as

$$P_\phi = V_{C\phi} I_{L\phi}, \qquad \phi \in \{a,b,c\}, \tag{8}$$

where $V_{C\phi}$ and $I_{L\phi}$ are the RMS filter-capacitor voltage and inductor current for phase ϕ. The maximum power deviation across phases is

$$\Delta P_{\max} = \max(|P_a - P_{\mathrm{avg}}|,\ |P_b - P_{\mathrm{avg}}|,\ |P_c - P_{\mathrm{avg}}|), \tag{9}$$

where $P_{\mathrm{avg}} = (P_a + P_b + P_c)/3$. Imbalance is flagged when $\Delta P_{\max}$ exceeds a threshold, typically 10–20% of rated power depending on load sensitivity.

C. Static Switch Control Logic

When imbalance is detected, the static switch transitions the system from three-wire to four-wire mode. A hold-off period (100–500ms) prevents nuisance switching. The neutral voltage and system fault status are verified before the switch closes. Switch closure is synchronized to the zero-crossing of the neutral current to minimize switching transients. After closure, neutral current is monitored to confirm successful four-wire operation. Switch opening follows the same logic in reverse, reverting to three-wire mode when the CUF and VUF return below threshold.

IV. Proposed Individual Phase Current Control Algorithm

A. Control Architecture Overview

The outer (voltage) loop operates in the synchronous D–Q frame to maintain balanced three-phase capacitor voltages. The inner (current) loop operates in the natural ABC frame for per-phase tracking with high bandwidth. The combined structure is shown in Fig. 2.

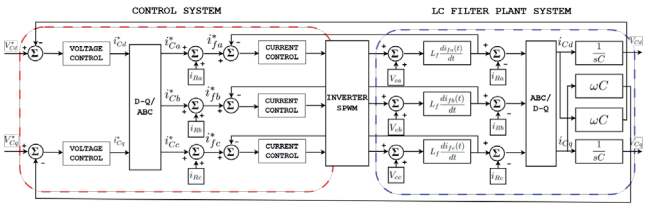

Fig. 2. Dual-loop control architecture: D–Q frame voltage controller (outer loop, red dashed boundary) and ABC frame current controller (inner loop) with load-current feedforward compensation.

The key design choices are: (i) D–Q frame voltage control for inherently balanced regulation; (ii) ABC frame current control for independent per-phase management without the zero-sum constraint of (4); (iii) explicit crosscoupling cancellation in the voltage controller; (iv) loadcurrent feedforward via (3) to improve transient response; and (v) bandwidth separation of at least 10:1 between the two loops.

B. D–Q Frame Voltage Controller

Applying the Park transformation to (3) yields the D–Q frame capacitor dynamics:

$$\begin{aligned} i_{Cd} &= C_f \dot{V}_{Cd} + \omega C_f V_{Cq}, \\ i_{Cq} &= C_f \dot{V}_{Cq} - \omega C_f V_{Cd}, \end{aligned} \tag{10}$$

where ω is the angular grid frequency and the crosscoupling terms $\pm\omega C_f V_{Cq,d}$ arise from the frame rotation. A PI controller with explicit cross-coupling cancellation generates the D–Q current references:

$$\begin{aligned} i^*_{Cd} &= \left(k_{pV} + \frac{k_{iV}}{s}\right)(V^*_{Cd} - V_{Cd}) + \omega C_f V_{Cq} \\ i^*_{Cq} &= \left(k_{pV} + \frac{k_{iV}}{s}\right)(V^*_{Cq} - V_{Cq}) - \omega C_f V_{Cd}. \end{aligned}, \tag{11}$$

With cross-coupling cancelled, the closed-loop voltage dynamics reduce to two decoupled second-order systems:

$$C_f \dot{V}_{Cd,q} = \left(k_{pV} + \frac{k_{iV}}{s}\right)\left(V^*_{Cd,q} - V_{Cd,q}\right). \tag{12}$$

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C. ABC Frame Current Controller with Feedforward

The current reference for each phase is obtained by inverse-Park transforming the D–Q references and adding the measured load current as a feedforward term derived from (3):

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$$i^*_{L,abc} = \mathbf{T}^{-1}_{dq\to abc}\left[i^*_{Cd},\ i^*_{Cq}\right]^\top + i_{R,abc}, \tag{13}$$

where $\mathrm{T}^{-1}_{dq\to abc}$ is the inverse Park transformation matrix. The feedforward term $i_{R,abc}$ makes the current reference respond immediately to load changes without waiting for voltage error to develop, which is the mechanism behind the fast settling times reported in Section VII.

A per-phase PI controller then tracks this reference:

$$v^*_{\mathrm{inv},\phi} = \left(k_{pI} + \frac{k_{iI}}{s}\right)\left(i^*_{L\phi} - i_{L\phi}\right) + v_{C\phi}, \quad \phi \in \{a,b,c\} \tag{14}$$

where the capacitor voltage $v_{C\phi}$ acts as a voltage feedforward to decouple the current loop from load-voltage disturbances. In four-wire mode, (14) is applied to each phase independently with no coupling between phases, as permitted by (5).

V. Stability Analysis and Controller Design

A. Small-Signal Modeling

The linearized closed-loop voltage-loop transfer function, obtained from (12), is

$$G_v(s) = \frac{\Delta V_{Cd}(s)}{\Delta V^*_{Cd}(s)} = \frac{k_{pV}s + k_{iV}}{C_f s^2 + k_{pV}s + k_{iV}}. \tag{15}$$

The linearized current-loop transfer function for each phase, from (2) and (14), is

$$G_i(s) = \frac{\Delta i_L(s)}{\Delta i^*_L(s)} = \frac{k_{pI}s + k_{iI}}{L_f s^2 + k_{pI}s + k_{iI}}. \tag{16}$$

Both transfer functions share the standard PI-controlled second-order form, which facilitates gain selection through pole placement.

B. Controller Parameter Design

Matching the denominator of (15) to a desired natural frequency $\omega_{n,v}$ and damping ratio ζ_v gives

$$k_{pV} = 2\zeta_v \omega_{n,v} C_f, \qquad k_{iV} = \omega_{n,v2} C_f. \tag{17}$$

The natural frequency $\omega_{n,v}$ is set to achieve a closed-loop bandwidth of 5–6 Hz. This value is chosen conservatively: it is high enough to regulate voltage against 50 Hz fundamental load variations, yet low enough to attenuate switching-frequency ripple and to remain well below the current-loop bandwidth, satisfying the stability separation requirement. A critical damping ratio $\zeta_v = 0.707$ $(1/\sqrt{2})$ is selected because it minimises settling time without overshoot, which is important for protecting sensitive loads [12].

Applying the same procedure to (16) yields the current controller gains:

$$k_{pI} = 2\zeta_i \omega_{n,i} L_f, \qquad k_{iI} = \omega_{n,i2} L_f. \tag{18}$$

The current-loop bandwidth $\omega_{n,i}$ is set to 1kHz (approximately 6283 rad/s). This value is selected to be 10–20× greater than the voltage-loop bandwidth, satisfying the bandwidth-separation criterion that ensures the inner loop tracks its reference before the outer loop generates a new one [13]. At 1kHz, the current loop is also well below the 20 kHz switching frequency, avoiding excitation of switching-frequency resonances. The same critical damping ratio $\zeta_i = 0.707$ is applied for consistency and to prevent resonant current peaking.

To verify robustness to filter parameter uncertainty, the gains are evaluated at nominal values and at ±20% of both L_f and C_f, as detailed in Section V-D.

C. Stability Under Three-/Four-Wire Transition

When the static switch closes and (4) is replaced by (5), the per-phase current controllers become fully decoupled. Since each phase controller (14) has the same structure and gains, stability is preserved across the transition and the only change is removal of the zero-sum coupling. The voltage controller (11) continues to operate unchanged in the D–Q frame; it sees the transition only as a load disturbance, which the feedforward path (13) immediately compensates.

D. Robustness to Parameter Variations

To quantify robustness, the closed-loop poles of $G_v(s)$ and $G_i(s)$ are evaluated when L_f and C_f deviate from their nominal values by ±20%, representing manufacturing tolerances, temperature drift, and ageing. Table I summarises the resulting closed-loop bandwidth and phase margin for each case.

Table I:
Closed-loop bandwidth and Phase Margin under fFilter Parameter Variations (±20% of Nominal L_f and C_f).

Case	L_f(mH)	C_f(µF)	BW_i(kHz)	PM_i(°)
Nominal	1.26	4.50	1.00	52
L_f–20%	1.01	4.50	1.25	49
L_f+20%	1.51	4.50	0.83	55
C_f–20%	1.26	3.60	1.00	52
C_f+20%	1.26	5.40	1.00	52
L_f+C_f+20%	1.51	5.40	0.83	55
L_f –C_f –20%	1.01	3.60	1.25	49

All cases maintain a phase margin above 45°, confirming adequate stability margin across the expected parameter range. The bandwidth-separation ratio between voltage and current loops remains above 10:1 in all cases. These results show that the proposed control design is robust to typical filter parameter uncertainties without requiring adaptive gain scheduling.

VI. Simulation Setup

A. System Parameters

All simulations were performed in PSIM with a detailed model comprising the three-level NPC inverter, L-C filter, proposed control algorithms, and load variations. Table II lists the simulation parameters.

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TABLE II
SIMULATION PARAMETERS.

Parameter	Value	Parameter	Value
V_{dc}	700[V]	C_f	4.5[μF]
R_L	30[Ω]	f_{PWM}	20[kHz]
L_f	1.26[mH]	P_{rated}	250[W/phase]
k_{pV}	0.0119	k_{iV}	0.0178
k_{pI}	11.21	k_{iI}	49.87 10^3

B. Test Scenarios

The system was implemented in three-phase four-wire configuration with the static switch short-circuited to allow per-phase current control throughout. Load variations were applied only to the R-phase to isolate the controller response to a single-phase disturbance while the other two phases remained undisturbed. Two scenarios were tested: (1) a 100% load increase (R-phase resistance halved at t = 0.5s) and (2) a 50% load decrease (R-phase resistance doubled at t = 0.5s).

VII. Simulation Results and Performance Evaluation

A. Load Increase Scenario

1) Without feedforward compensation: Fig. 3 shows the system response without feedforward. Despite the load doubling, current increased by only 0.8A, well below the 1.76A required to match the new load. The resulting Rphase voltage drop created visible three-phase voltage imbalance while the other two phases remained near nominal.

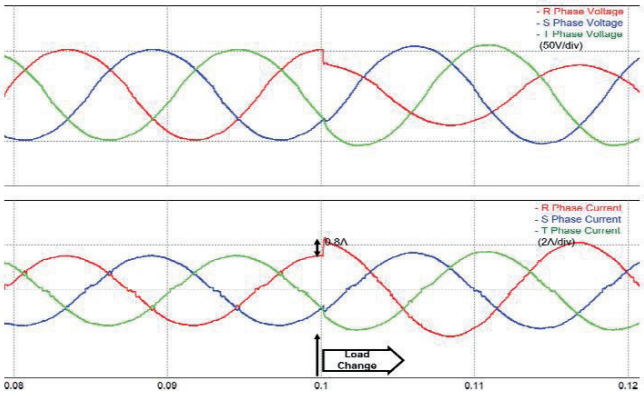

Fig. 3. Capacitor voltage and inverter current *without* feedforward: 100% load increase on the R-phase.

2) With feedforward compensation: Fig. 4 shows the compensated response. Current increased by 1.76A, closely matching the doubled load. The feedforward term supplied the current reference before voltage could deviate appreciably. All three phase voltages remained balanced, and steady-state conditions were re-established within approximately three fundamental cycles.

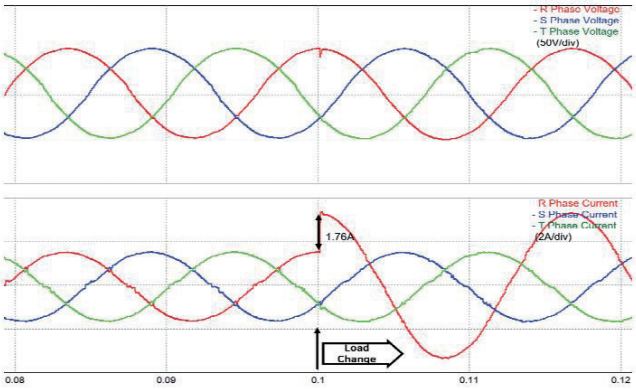

Fig. 4. Capacitor voltage and inverter current *with* feedforward: 100% load increase on the R-phase.

B. Load Decrease Scenario

1) Without feedforward compensation: Fig. 5 shows the response to a 50% load decrease without compensation. Current reduced by only 0.5A while the load required a 1.02A reduction. The excess current caused the Rphase voltage to rise, introducing imbalance and potential overvoltage stress.

2)With feedforward compensation: Fig. 6 shows the compensated response. Current decreased by 1.02A, accurately matching the reduced load, and peak-to-peak ripple fell by approximately 40%. All three phase voltages relationships. The system settled within roughly two fundamental cycles.

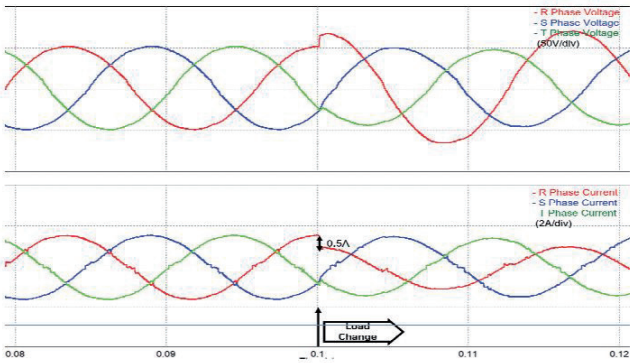

Fig. 5. Capacitor voltage and inverter current *without* feedforward: 50% load decrease on the R-phase.

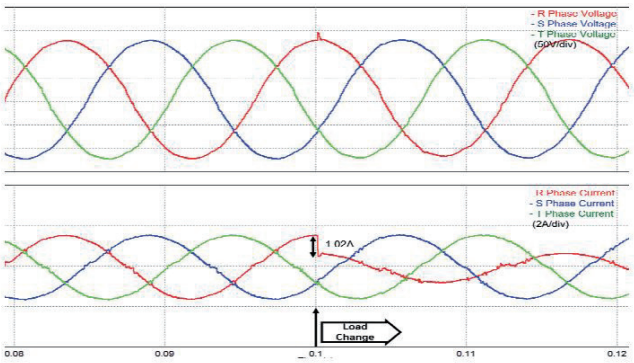

Fig. 6. Capacitor voltage and inverter current *with* feedforward: 50% load decrease on the R-phase.

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C. Harmonic Distortion Analysis

Fig. 7 shows the inverter output current spectrum from DC to 3kHz (up to the 50th harmonic at 60Hz fundamental).

Without compensation, THD reached 13.18%, exceeding the IEEE 519 limit of 5%. Pronounced low-order harmonics were present: the 3rd at 8.5%, 5th at 6.2%, and 7th at 4.8% of the fundamental. With compensation, THD dropped to 3.64% (a 72.4% reduction), satisfying the IEEE 519 requirement. The 3rd, 5th, and 7th harmonics fell to 2.1%, 1.5%, and 1.0%, respectively.

Beyond THD, Table III reports three additional distortion indices to provide a more complete picture of power quality.

The crest factor (CF), defined as the ratio of peak to RMS current, falls from 1.81 to 1.43 with compensation, indicating a more sinusoidal waveform with lower peak stress on switching devices. THD_I (current THD referenced to the fundamental component rather than to the total RMS) follows the same trend as THD. The VUF, computed from (7), drops from above 8% to below 1%, confirming that the proposed algorithm effectively restores voltage balance in addition to reducing harmonic content.

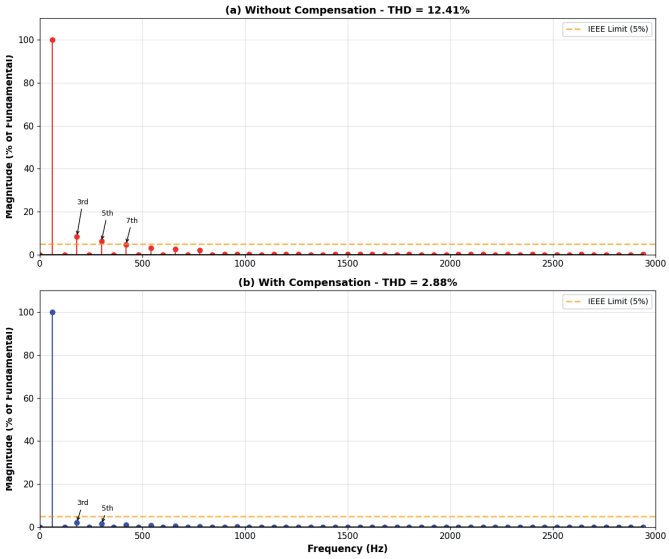

Fig. 7. Inverter output current harmonic spectrum: (a) without compensation (THD=13.18%), (b) with compensation (THD=3.64%). The orange dashed line indicates the IEEE 519 limit of 5%.

TABLE III:
Harmonic distortion indices: without vs. with feedforward compensation.

Index	Without comp.	With comp.
Total harmonic distortion (THD)	13.18%	3.64%
Total harmonic distortion of current (THD_I, fundamental-referenced)	12.95%	3.51%
Crest factor (CF)	1.81	1.43
Voltage imbalance factor (VUF)	>8%	<1%

VIII. Comparative Performance Evaluation

Table IV summarises the main performance differences between the uncompensated and compensated methods.

The compensated system achieves current tracking errors below 2%, VUF below 1%, and settles approximately three times faster than the uncompensated approach. The per-phase feedforward, enabled by four-wire reconfiguration, allows each phase to be adjusted independently without disturbing the other phases—a fundamental capability that conventional three-wire D–Q methods cannot replicate.

IX. Practical Implementation Considerations

Several aspects deserve attention when moving from simulation to hardware. The feedforward path requires high-bandwidth current sensors with low phase delay to keep load current measurements accurate at the 1kHz current-controller bandwidth. Anti-aliasing filters must suppress measurement noise without introducing phase shift that could destabilise the current loop. A DSP or FPGA with sufficient throughput is needed to execute both coordinate transformations, the three PI controllers, and the feedforward calculation within each sampling interval; a sampling rate of at least 10–20kHz is recommended.

The static switch must be rated for the expected neutral current and capable of efficient continuous operation in four-wire mode. Gate drivers should provide fast, reliable switching synchronised with the imbalance detection output. The control software should incorporate overcurrent detection, overvoltage monitoring, and thermal management, along with graceful degradation strategies if a sensor or computational resource becomes temporarily unavailable.

Table IV
Performance Comparison: Uncompensated vs. Compensated Control.

Metric	Without compensation	With compensation
Current tracking error (load increase)	>60%	<2%
Current tracking error (load decrease)	>50%	<2%
Voltage imbalance factor (VUF)	>8%	<1%
THD	13.18%	3.64%
Crest factor (CF)	1.81	1.43
Settling time	8–10 cycles	2–3 cycles
Ripple current reduction	—	40%

X. Conclusions

This paper proposed an individual phase current control (IPCC) algorithm with load-current feedforward compensation for maintaining stable, balanced voltages during islanding under severe imbalanced loading. The dualloop architecture separates voltage regulation (D–Q frame, 5–6Hz bandwidth) from current tracking (ABC frame, 1kHz bandwidth), combining the symmetry advantages of synchronous-frame control with the per-phase flexibility of natural-frame control.

The explicit novelty—ABC-frame feedforward combined with automatic three-/four-wire reconfiguration— removes the zero-sum constraint in three-wire mode and allows each phase current to be updated instantaneously on a load disturbance, before

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voltage error can develop. This mechanism reduces tracking error from over 50–60% to below 2%, reduces THD from 13.18% to 3.64% (satisfying IEEE 519), and reduces settling time from 8–10 cycles to 2–3 cycles. Robustness analysis confirms phase margins above 45◦ across ±20% filter-parameter variations.

Future work will address experimental validation on a hardware prototype, performance under mixed resistive– inductive and nonlinear loads, adaptive gain scheduling for varying load compositions, and coordinated protection schemes for fault scenarios during extended islanding.

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