ISSN 0005–1144
ATKAAF 47(1–2), 59–67 (2006)

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ADSL Analog Front End

UDK 621.395.345
004.716
IFAC 4.5.2;5.8.6

Review

In this paper the Asymmetric Digital Subscriber Line (ADSL) analog front end (AFE) designs are described and compared. AFE is the part of ADSL modems most responsible for quality signal transmission over phone wires. It can be divided into the transmitting path (TX) circuitry, the receiving path (RX) circuitry and the hybrid network and transformer. The operations and realizations of each functional block are presented. There are the D/A converter, the filter and the line driver in the TX path and the voltage gain amplifier, the filter and the A/D converter in the RX path. The hybrid network and transformer process signals in both directions. Different fabrication technologies are used for the practical realizations of the AFE chip. The directions of the further developing are notified.

Key words: analog filter, asymmetric digital subscriber line, broadband communications, data converters, line driver, wireline access

1 INTRODUCTION

Asymmetric Digital Subscriber Line (ADSL) technology is one of the broadband communication systems which allows us to get digital services in our homes. It uses copper twisted pair wires, spread all over the world, primary installed for phone connections, over distances of 1.5–6 km [1–12].

ADSL operates with passband modulation using a frequency spectrum of 25 kHz–1.1 MHz. The transmission speeds are 1.5–8.5 Mbps downstream and 16–640 kbps upstream. Downstream (DS) means traffic from the Central office (CO) to the Customer's premises (CP) and upstream (US) is vice versa, from the CP to the CO. The speed represents the bit rate and is expressed in bits per second (bps).

This technology intends to replace today most spread ISDN connections, which can run at a maximum speed of 144 kbps, so it represents a great step forward. Services, such as video-on-demand, digital TV, teleshopping and the most popular Internet, by their nature require asymmetric communication. Teleconferencing and distance learning as symmetric communication services can also be transmitted by ADSL technology. ADSL is, based on the today available infrastructure, the best solution to get it. There are others xDSL technologies but for now ADSL is the most promising one.

Research on this technology started in the early 90's when the first papers were published. Implementation in everyday life started ten years later. Improvements are made almost every year to establish a safe way of digital communication. In this paper, a part of ADSL architecture will be presented, the part that demands the most careful design for proper operation and quality signal transmission.

2 ADSL TECHNOLOGY

ADSL communication path between the CO and the CP is shown in Figure 1. As can be seen, it allows phone/fax service using a signal splitter. Two additional hardware units need to be installed, an ADSL transmission unit at the Central office (ATU-C) and an ADSL transmission unit at the Customer's premises (ATU-R, letter R means remote side).

Several vendors today deliver compatible equipment for this purpose. The frequency spectrum of ADSL transfer is shown in Figure 2. The range 0–4 kHz is reserved for phone service (Plain Old Telephone Service – POTS). Upstream communication uses the 25–128 kHz range and downstream takes the whole 25 kHz–1.1 MHz band.

As DS and US bands overlap, an echo cancellation technique must be implemented. ADSL uses a Discrete Multitone (DMT) modulation technique where the whole bandwidth is divided into 256 subchannels of 4.3125 kHz each. The signal in each channel is QAM modulated. After coding, obtained by combining Trellis coding and interleaved Reed-

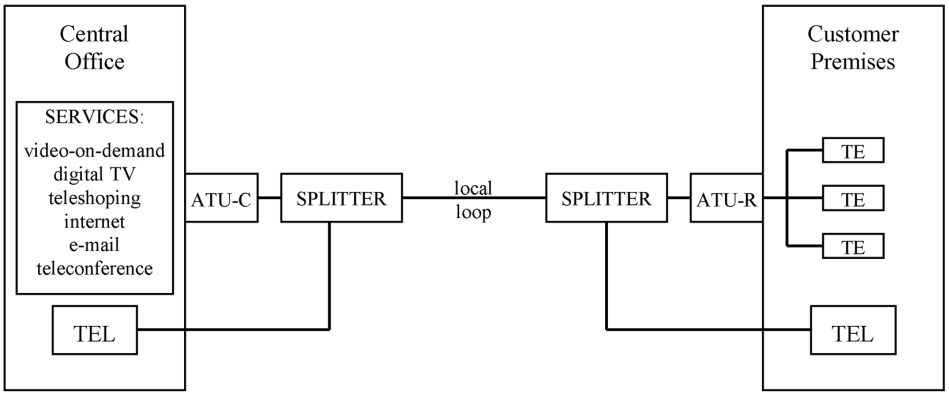

Fig. 1 ADSL »last mile« communication path between the CO and the CP

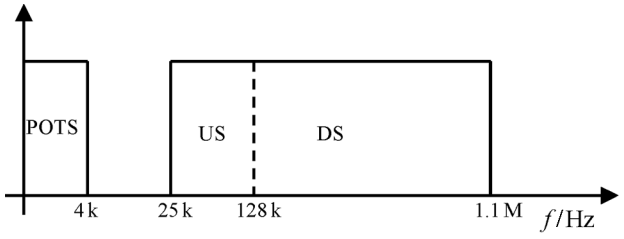

Fig. 2 ADSL frequency spectrum

-Solomon coding with forward error correction, the signal is modulated [3–5, 13]. Those actions are done in the digital interface part. Leaving the digital interface, the signal enters the analog interface also called the analog front end. The next paragraph describes what happens there.

3 ANALOG FRONT END

The block scheme of an AFE is presented in Figure 3. For proper understanding, in the picture the preceding digital interface and the succeeding transmission line are also shown. It was said earlier that coding and modulation are done in the digital interface by digital signal processing.

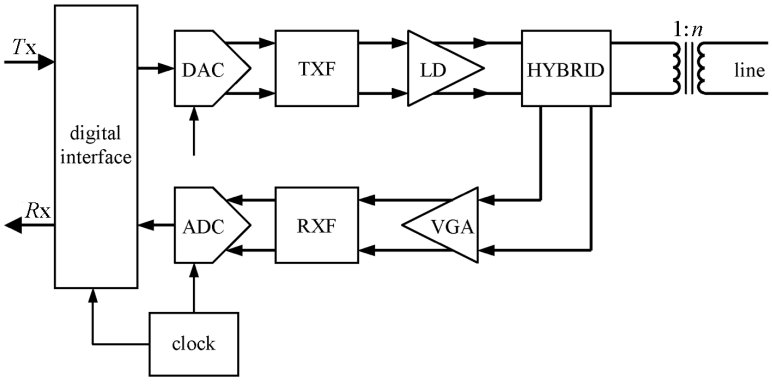

Fig. 3 ADSL AFE functional blocks scheme

The analog interface accepts digital data from various services, performs the previously mentioned operations and delivers a digital signal to the analog interface. In the opposite direction, it receives an analog signal, performs demodulation and decoding and sends information to the services. Analog signal processing is done in the analog front end. It consists of three operating paths: a transmitting path, a receiving path and a hybrid network with transformer as a bidirectional path. The clocking system is also shown and it supports data converting blocks in both paths.

3.1 Transmitting path (TX)

This path consists of three functional blocks: a digital to analog converter, a filter and a line driver. Their function and design will be described in the next paragraphs. To increase the dynamic range all blocks are designed in fully differential versions, as are the blocks in the receiving path.

3.1.1 D/A converter (DAC)

The first operation that should be done in the AFE is the digital to analog conversion. This is the task of the D/A converter. As for any other block, there are several DAC designs that are different in resolution and realization. However, common to all is that they use current steered technology as the best one for resolution and speed.

One of them is the 14-bit 5-MHz current steered D/A converter [14]. Four MSBs and ten LSBs are processed separately and connected at the output of DAC. There is also feedback implemented in that system to establish the full-scale output current. The circuit operates at ±5 V supply.

The next one operates at 3.3 V supply [15]. It is also current steered but a 12-bit DAC with an 8.816 MHz sampling rate. The bits are separated in an 8 MSBs group and a 4 LSBs group. It has lower resolution than the previous one but also reduced power.

The DAC presented in [16] has increased resolution to 16-bit at 8.832 MHz. It uses a switched capacitor digitally calibrated multistage architecture with a 5 V supply. Resolution is increased and the power too.

A low power, 3.3 V supply circuit is described in [17]. It is a 14-bit, 13.2 MHz fully differential current steered circuit. This design represents the best trade-off in resolution and power.

A 12-bit 17.664 MHz DAC with improved linearity is presented in [18]. It uses four banks of current sources with programmable output current from 1–10 mA. Bits are again separated into MSBs and LSBs groups. At the output is, as for the most of previous designs, a summing amplifier, which converts current to the fully differential voltage. If not, then this conversion is done in the following filter [14]. A summary of the presented DAC is given in Table 1.

Table 1 **Properties of presented DACs**

Design	Supply	Resolution	Frequency
[14]	±5 V	14 b	5 MHz
[15]	3.3 V	12 b	8.816 MHz
[16]	5 V	16 b	8.832 MHz
[17]	3.3 V	14 b	13.2 MHz
[18]	3.3 V	12 b	7.664 MHz

3.1.2 TX Filter (TXF)

The purpose of this filter is to reject the image after the D/A conversion and reduce the noise. Filters in the transmitting and receiving paths aren't, in general, the same design. In designing such filters special care should be taken with linearity. There are several types of filter orders and approximation characteristics which are used in design. But all of them are active RC designed, because of the demand for high linearity.

Transmitting path filters are usually low pass (LPF) third [14] or fourth [15, 16], order filters with Butterworth [16] or Chebyshev [14, 19] approximation functions. Practical designs vary. In [14], a Rauch biquad is used to implement the second order section, Figure 4. It minimizes the number of operational amplifiers what leads to reducing power and decreasing the noise and distortion. The cut-off frequency is set to 1.1 MHz.

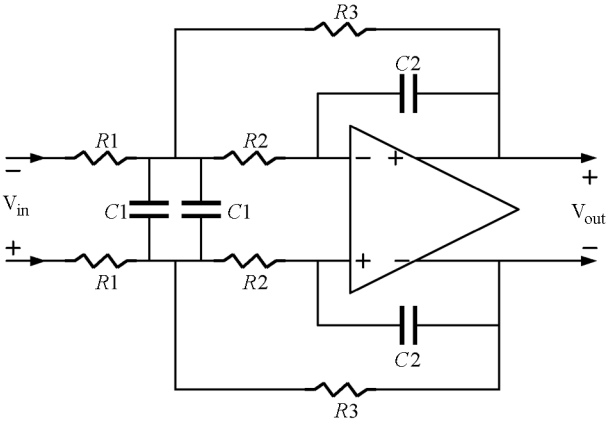

Fig. 4 Rauch biquad as a second order low pass filter

In [15], the leapfrog topology is used to obtain high linearity and a wide tuning range.

A cascade of two 2nd order sections to realize the 4th order filter is shown in [16]. Cut-off frequencies are set to 1.1 MHz for ATU-C or 138 kHz for ATU-R devices.

A combination of a 3rd order Chebyshev low pass filter with a cut-off frequency of 1.3 MHz and a 0.25 dB pass-band ripple with a 3rd order Chebyshev high pass filter with a cut-off frequency of 155 kHz and a 0.25 dB ripple is proposed in [19]. The overall transfer function of the filter in the transmitting path is in this case a pass band type.

An interesting combination of filters is proposed in [18]. In the transmitting path is combination of a 4th order elliptic 1.1 MHz cut-off frequency low pass filter and a 3rd order elliptic 138 kHz cut-off frequency high pass filter. These filters are designed using signal flow graph methods and simulate the operation of LC prototypes.

A summary of the filter's characteristics is given in Table 2. Almost all filters provide automatic tuning to avoid errors due to the fabrication process. These schemes usually set the cut-off frequency inside 5 % of the nominal value and Q-factors inside 10 % of the nominal value.

Table 2 **Properties of presented TX filters**

Design	Type	Order	Supply	Cutt-off frequency
[14]	LP-Chebyshev	3rd	±5 V	1.1 MHz
[15]	LP	4th	3.3 V	1.1 MHz
[16]	LP-Butterworth	4th	5 V	1.1 MHz
[18]	LP-Elliptic HP-Elliptic	4th 3rd	3.3 V	1.1 MHz 138 kHz
[19]	LP-Chebyshev HP-Chebyshev	3rd 3rd	N/A	1.3 MHz 155 kHz

3.1.3 Line Driver (LD)

The line driver is the most challenging part in AFE design and more papers are published on that part than other parts of AFEs. Designs vary much more widely than other AFE system blocks. The line driver determines the final signal which goes to the transmission line, the copper twisted wire.

The ADSL standard requires 20.4 dBm average power on the 100 Ω phone line (110 mW or 3.31 V_{rms} differential). The problem is in the nature of DMT modulated signals, Figure 5. This waveform is the result of a combination of 224 Quadrature Amplitude Modulated (QAM) signals in each subchannel.

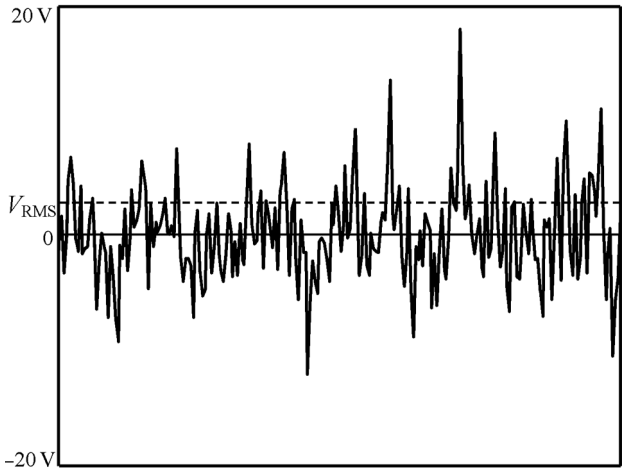

Fig. 5 DMT time domain signal scaled on the line values

The peaks occur when many of the subchannels are aligned in phase. Peak voltage can be 6 times higher than average, which gives a 19.86 V_p differential. It leads to a ±10 V voltage supply which is very inefficient due to a high loss of power because of high quiescent currents in the LD amplifier. This problem is the main reason for a fully differential analog circuit design. In common mode circuits ±20 V voltage supply should be used which will waste more power. However, on one side the output voltage of the line driver is decreased using a line transformer and on the other side there are losses on termination impedance that increase LD output voltage. To reduce these losses, active termination is performed on the line drivers. And again, there is a trade off because active termination will decrease the incoming signal from the line. In addition, some LD designs are discussed.

The first line drivers were built with discrete components due to a higher voltage supply than digital and other analog circuits require [15, 16]. Designers often place the LD out of the AFE because the rest of the AFE is integrated in the same chip. As technology goes into the submicron region, the power supply level also goes down. Instead of a line driver, AFE TX path usually ends with a programmable amplifier (PA) as a forestage to a discrete LD.

The next step in LD development was the integration into the AFE. Line drivers with active termination reduce LD output voltage and therefore it becomes available for integration. There are different types of LDs based on the output stage [20]. Most used is the class-AB output stage [17, 19, 21, 22]. Different designs use different power supplies, a single 12 V supply is used in [17], a single 15 V in [19], a ±12 V in [21] and a single 5 V in [22]. Various design techniques are used to improve LD properties. Power saving using single active termination is done in [21]. Digital control of the quiescent current is performed in [22] and offers a good compromise of power consumption and linearity.

Improved power efficiency produces the class-H LD presented in [23–25]. This design uses an AC power supply where the supply level is adjusted to the input signal level. The nominal DC supply is ±6 V in [23], a single 12 V in [24] and ±3 V in [25] but using the proposed supply method, the required output signal swing could be achieved. There is a sensing block and charge pump which raise and drop the power supply level. The basic operation scheme is shown in Figure 6.

Two different power supplies provides class-G output stage and it is used in [26]. The output stage is alternatively connected to one of them depending on the signal level. For signals lower than the reference level a lower supply is used and for higher signals the supply is switched to a higher supply. There can be problems with signal distortion due to switching at higher frequencies but by using the proper technique this can be avoided. A low power

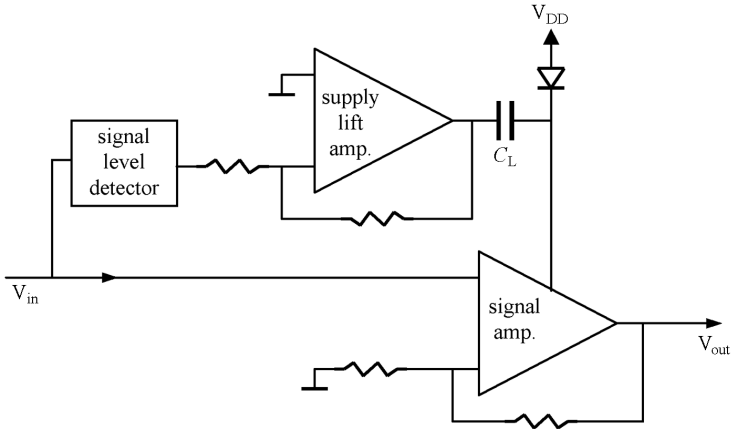

Fig. 6 Class-H line driver half-circuit power supply scheme

class-G LD obtained with zero-overhead solution is shown in [26].

Some special designs are presented in [27] and [28]. The self-oscillating power amplifier technique presented in [27] gives asynchronous switching amplifier in the LD which provides low distortion and high efficiency for DMT signals. Another approach presented in [28] uses high voltage (30 V) but due to the circuit design, produces only 1 mA quiescent current. There are some papers that can help readers in line driver design [29–31]. A summary of the presented line drivers is given in Table 3.

Table 3 **Properties of presented line drivers**

Design	Output stage class	Supply
[17]	AB	12 V
[19]	AB	15 V
[21]	AB	±12 V
[22]	AB	5 V
[23]	H	±6 V
[24]	H	12 V
[25]	H	±3 V
[26]	G	5 V/15 V
[28]	N/A	30 V

3.2 Receiving path (RX)

This part of the AFE also consists of three functional blocks and those are the voltage gain amplifier, the filter and the analog to digital converter. The function and design of all of them will be described in the next paragraphs. To increase dynamic range, as in the TX path, all blocks are designed in fully differential versions.

3.2.1 Voltage gain amplifier (VGA)

As the last component in TX path, the line driver, is a critical one for quality transmission, here this responsibility lies on the input voltage gain amplifier. Some authors use the term low noise amplifier (LNA) or programmable gain amplifier (PGA) but the purpose is the same: a weak signal at the end of the line should be amplified to the voltage level required at the filter input. The line attenuation, where typical parameters of phone wires in frequency range over 100 kHz are $k_R = 0.2$, $L = 0.6$ mH/km and $C = 0.05$ μF/km [32], is shown in Figure 7.

It can be seen that for longer distances (6 km) attenuation of the signal is almost –120 dB. It means that at that point, the line driver average output signal of 10 dB (3.31 V) will appear as 3.2 μV. To avoid that situation, the lower part of the spectrum

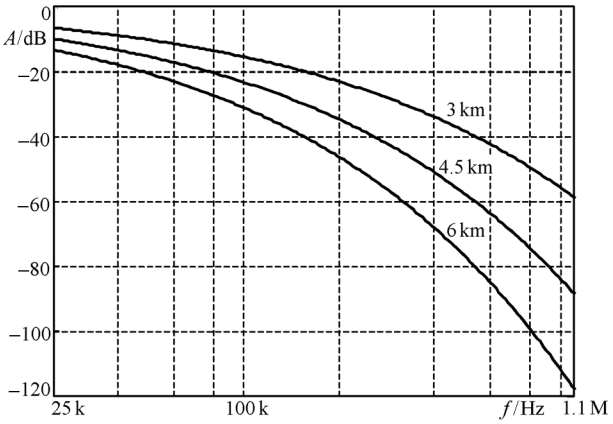

Fig. 7 Line attenuation in the ADSL frequency spectrum

is used for more traffic. However, standard allows 6 km line lengths and specifications have to be met. Because of the wide scale of input voltages, which is a function of frequency and distance (Figure 7), the VGA should have programmable gain. The main problem in VGA design is the need to achieve low input noise. In [14] VGA is performed using a discrete receiving amplifier and two stages integrated in the AFE. The first one is a high impedance with 12 nV/$\sqrt{\text{Hz}}$ referred input noise and gain 0–24 dB. The second stage fits the signal into the following block dynamic range. The VGA presented in [15] is also split into discrete and integrated components. The low noise amplifier has 0–31 dB programmable gain with 1 dB steps and the same noise floor as the previous one. Two stages are also used in [18] where the first stage has a gain range –6 to 24 dB with 3 dB granularity and the second stage has a gain range of 0–23 dB with 1 dB granularity.

A summary of the presented VGAs is given in Table 4. In different AFEs, voltage gain amplifier designs are not as different as line driver designs. There are only variations on the basic VGA scheme. Depending on the technology used, the gain range and noise are set to obtain the maximal dynamic range of the VGA.

Table 4 **Properties of presented VGAs**

Design	Supply	Gain	Input noise
[14]	±5 V	0–24 dB	12 nV/$\sqrt{\text{Hz}}$
[15]	3.3 V	0–31 dB	12 nV/$\sqrt{\text{Hz}}$
[18]	3.3 V	–6 to 24 dB	N/A

3.2.2 RX Filter (RXF)

The purpose of this low pass filter is an antialiasing function prior to A/D conversion. They are also third [18] or fourth [19] order filters with Butterworth or Chebyshev [19] approximation functions.

RX filters are designed with a unity gain or a small gain (up to 6 dB) to adjust the dynamic level to ADC.

In some AFE designs, the RX filter is the same topology as theTX filter [14, 16, 17]. In [18] is proposed a 3rd order elliptic low pass filter with 138 kHz cut-off frequency. It is also implemented with an RC active section. Switch-capacitor topologies are not suitable in ADSL AFEs because of demands for high linearity. Such specifications can be met with active RC filters or recently proposed OTA-C filter topology [33]. Besides the filtering function, in [33] there is also designed a variable gain in the filter structure.

3.2.3 A/D converter (ADC)

The last operation that should be done in the receiving path is digital to analog conversion. From three types of A/D converters, which are subranging flash, sigma-delta and pipelined, the last one is the most used in the AFE design [15, 16, 18].

A 13b resolution ADC and 8.816 MHz (MHz is equivalent to MSamples/s) sampling rate using redundancy combined with digital error correction is proposed in [15]. In this case the oversampling rate is 4×. A block scheme of ADC architecture is shown in Figure 8.

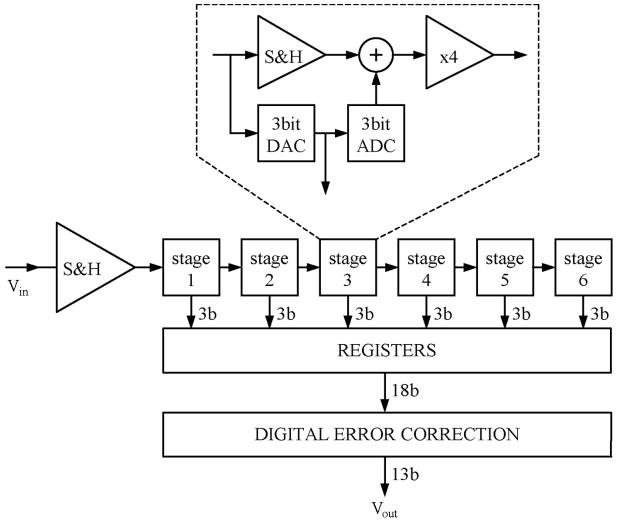

Fig. 8 Pipelined ADC architecture

A higher 16b resolution provides a switched-capacitor digitally calibrated multistage pipeline structure with a high gain OTA presented in [16]. It minimizes calibration drift over temperature. The sampling rate is 4.416 MHz or 2.208 MHz. Lower 12bits resolution is obtained in [18] where current scaling is implemented along the stages, so power is reduced.

Another approach in ADC design is proposed in [17] using a sigma-delta technique. A 14b converter is realized operating at 26 MHz with an oversampling rate of 12×. Switched-capacitors and OTA are used in realization and no calibration in this case is needed. A summary of the presented ADCs is given in Table 5. Digital calibration of ADC is not needed if the capacitor matching is good enough. If not, offline or online calibration should be implemented. Offline calibration requires a simple digital circuit but sometimes is not possible, depending on circuit requirements. Online calibration needs a redundant stage, which allows large spending on area and power.

Table 5 **Properties of presented ADCs**

Design	Type	Supply	Resolution	Frequency
[15]	pipelined	3.3 V	13 b	8.816 MHz
[16]	pipelined	5 V	16 b	4.416 MHz
[17]	sigma-delta	3.3 V	14 b	26 MHz
[18]	pipelined	3.3 V	12 b	7.664 MHz

3.3 Hybrid network and transformer

The hybrid network provides a bidirectional path. It leads the signal from the line driver to the line and blocks this signal into the receiving path allowing the incoming signal to reach the voltage gain amplifier. This network, combined with a transformer, also provides a proper termination of the line. The 2*R*-*R* network for passive termination is presented in Figure 9.

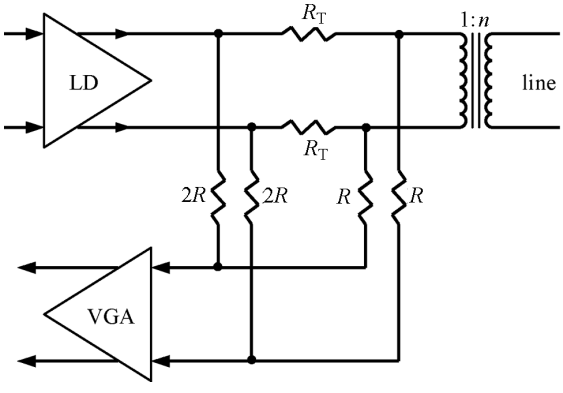

Fig. 9 Hybrid network and transformer scheme

Resistors R_T are termination resistors and they are equal to one half of line impedance scaled with n^2 where n is the transforming factor. But in practice, finite LD output impedance placed in series with $2R_T$ has to be taken into account, which will slightly decrease the previous value. Another impedance network for more accurate termination can

also be set [20]. With short network analysis, it is clear that half of LD output voltage is dropped on termination resistors and because of that half of the delivered power is wasted. As explained before, due to the high crest factors of the DMT signal, the output voltage of the LD is already high. To decrease this value the transformer is used. Different designs use different ns and in literature it is taken from 1.1 [24] over 2 [17, 23], 2.7 [25] to 4 [22]. Nevertheless, as much as LD output voltage is decreased using a higher transforming factor, the input signal of VGA is also decreased for the same value.

Active termination is also a method used to decrease power wasting. With additional resistors properly placed over the LD, the output impedance of the LD looks higher from the transformer side [34, 35]. That does scaling of termination resistors by factor α. And again, as LD voltage is decreased the input signal of the VGA is also decreased for the same value.

The hybrid network is recently realized in integrated CMOS technology and the transformer is still realized discretely, out of the AFE chip. Proper termination is not easy to design. CMOS process tolerances will result with non-calculated resistor values and line impedance is variable depending on wire type and signal frequency. On both sides of the termination equation are unpredictable factors. Because of that, some designs use adaptive line driver output to match transformed line termination [30, 31].

4 DISCUSSION

Corner values for transmission quality are given by standards [36, 37]. Power spectral density (PSD) mask, return and insertation loss and noise density are some of this parameters. One of the most important factor is the Missing Tone Power Ratio (MTPR). It provides the information of how much the signal is above the noise on the output of the LD.

Although in previous paragraphs the analog front end is treated as a uniform device, there are in practice different designs for the CO and the CP sides. In the CO the main design factors are power consumption (heating) and area (many users), and in CP design the dominant factor is price. The analog circuit design is always a trade-off between several factors: power – linearity – dynamic range – die area. The designer must take from something to give to another and in that process specifications must be fulfilled. On designer is to choose technology for AFE integrated circuits chip. It is well known that technology reaches more and more into the submicron region (also called nanotechnology).

The presented block designs are various. Some blocks have slightly different designs (DACs and VGAs), others have several versions (filters and ADCs) and finally the LDs could have completely different designs. There is no unique answer as to which presented design is the best, one has the lowest power consumption, another has the highest MTPR, another has the smallest die area or is the cheapest one. In Table 6 some AFE realizations are compared.

Table 6 **The AFE design parameters**

Design	Technology	Die area	Power	MTPR
[14]	1.2 μm BiCMOS	25.8 mm^2	750 mW without LD	65 dB
[16]	0.5 μm CMOS	32.8 mm^2	825 mW	81 dB
[17]	0.6 μm BiCMOS	29 mm^2	800 mW	80 dB
[19]	Bipolar SOI	N/A	N/A	74 dB

Several technologies are used for the fabrication of the AFE chip. From the first dimensions of 1.2 μm today's models use 0.25 μm or even 0.18 μm technology. Bipolar, complementary Bi-CMOS or CMOS technologies are used to obtain desired characteristics. Any combination of dimensions and process has its own price, which is also an important factor in AFE design.

5 CONCLUSION

ADSL technology is both the present and the near future in digital communications over telephone wires. This technology gives higher speed in data transmission and improves the quality of the received services. The most dominant part in defining that quality is the analog front end, the part which deals with signals on the lines. Analog signal processing is very sensitive to non-idealities and that design must be done as accurately as possible. That differentiates one designer from another.

There is continuing improvement in ADSL standards [38, 39]. The specifications become sharper and the AFE must follow them. Another design direction is to decrease power and area which will decrease the overall price of ADSL equipment and therefore make it more accessible to consumers. In that chain, more consumers will then decrease central office setup costs and further decreases in ADSL deployment is accomplished. Of course, there is some cost limit but it is an affordable limit to ordinary customers. Therefore, we are entering the information future and ADSL AFE design is just a small, but important part of that.

ACKNOWLEDGEMENT

This work is supported by Croatian Ministry of Science and Technology under grant 0069015 and Fulbright grant, year 2003. Work is done at Texas A&M University, Department of Electrical Engineering, Analog and Mixed Signal Center in College Station, Texas.

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ADSL analogno sučelje. U radu su opisane i uspoređene izvedbe ADSL analognog sučelja. Analogno sučelje kao dio ADSL modema najodgovornije je za kvalitetan prijenos signala preko telefonskih žica. Može se podijeliti u sklopove predajnog puta, prijamnog puta i hibridnu mrežu s transformatorom. Prikazan je rad i izvedbe svakog funkcijskog bloka. To su D/A pretvornik, filtar i izlazno pojačalo u predajnom putu te ulazno pojačalo, filtar i A/D pretvornik u prijamnom putu. Hibridna mreža i transformator prosljeđuju signale u oba smjera. Za praktičnu izvedbu AFE čipa koriste se razne tehnologije. Naznačene su smjernice daljnjeg razvoja.

Ključne riječi: analogni filtar, izlazno pojačalo, pretvornici signala, simetrična digitalna pretplatnička linija, širokopojasne komunikacije, žičani pristup

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Received: 2006-03-30