Power Loss Minimizing Control of Cascaded Multilevel Inverter with Efficient Hybrid Carrier Based Space Vector Modulation

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Abstract *– This paper presents a power loss minimization technique for a cascaded multilevel inverter using hybrid carrier based space vector modulation. The proposal in this paper combines the features of carrier based space vector modulation and the fundamental frequency modulation strategy. The main characteristic of this modulation is the reduction of switching loss and energy efficiency improvements with better harmonic performance. In order to implement this hybrid modulation scheme and deliver the hybrid PWM pulses to the appropriate switches, a TMS320F2407 digital signal processor (DSP) and a Complex Programmable Logic Device (CPLD) are used. The inverter offers lower harmonic distortion and operates with equal thermal stress among the power devices. Using simulation and experimental results, the superior performance of a new PWM method is shown.*

Keywords *– carrier-based space vector modulation, cascaded multilevel inverter, digital signal processor, power loss analysis, total harmonic distortion*

1. INTRODUCTION

Multilevel pulse width modulation inversion is an effective solution for increasing power and reducing harmonics of AC waveforms. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage is decreased due to a lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained [1]. Various multilevel converter structures are reported in the literature, and the cascaded multilevel converter appears to be superior to other multilevel converters in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter [2]. The power circuit for a five-level cascaded inverter topology shown in Fig.1 is used to examine the proposed PWM technique.

Modulation control of any type of a multilevel inverter is quite challenging, and much of the reported research is based on somewhat heuristic investigations. Switching losses in high power converters represent an issue and any switching transitions that can be eliminated without compromising the harmonic content of the final waveform are considered advantages [3]. Most of the modulation methods developed for multilevel inverters is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition PWM), or with horizontal displacements (phase-shifted PWM) [4].

Space-vector modulation is also extended for the multilevel inverter operation [5]. These high frequency methods produce high frequency stepped voltage waveforms that are easily filtered by the load and, therefore, they present very good reference tracking and low current harmonic distortion. However, this is also the reason for high switching losses, which is undesirable in high-power applications. As a result, low-frequency methods have been presented.

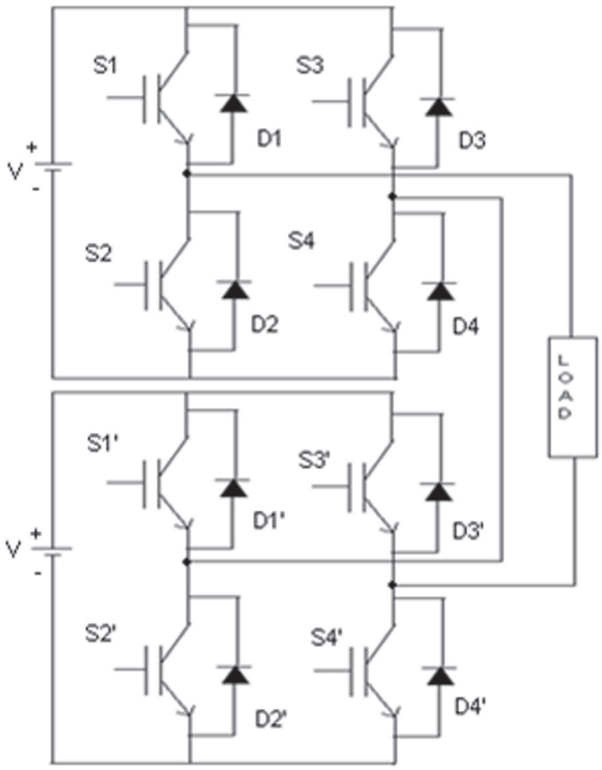


Fig. 1. Schematic diagram of the inverter topology (one phase leg) used to verify the proposed five-level hybrid carrier based space vector modulation.

Multilevel space-vector control reduces switching losses but has a variable magnitude error for the fundamental component [6]. Selective harmonic elimination (SHE) is also extended for multilevel inverters [7]. Nevertheless, offline calculations are necessary, making dynamic operation and closed loop implementation not straightforward. In addition, selective harmonic elimination becomes unfeasible with the increase of the number of levels, since it is directly related to the number of angles, hence equations that need to be solved. Carrier based space vector modulation was developed first for bipolar PWM and then extended to a multilevel inverter [8]. Wenxi Yao proposed that these techniques are harmonically equivalent, with the best spectral performance being achieved when the nearest three space vector states are selected with the middle two vectors centered in each half carrier switching interval [9]. This strategy is known as carrier based space vector modulation (CBSVM).

In this paper, a new modulation technique is presented to addresses reduction of switching losses in a cascaded multilevel inverter, with an improved harmonic performance. This modulation is a combination of fundamental frequency modulation and carrier based space vector modulation. The paper is organized in the following way. Section 2 describes carrier based space vector modulation suitable for the cascaded multilevel inverter. The proposed hybrid carrier based space vector modulation is discussed in detail in Section 3. Section 4 presents power loss minimizing control and an analysis of a cascaded multilevel inverter with this proposed modulation. Section 5 illustrates simulation and experimental results of different operating points including the discussion on the results. Finally, some conclusions are presented in Section 6.

2. REVIEW OF CARRIER BASED SPACE VECTOR MODULATION

Space vector modulation (SVM) offers low harmonic distortion for three phase inverters by placing the most unwanted harmonics power on triplen harmonics. SVM is intrinsically a non-carrier based digital technique for generating switching angles. However, due to a constant sampling rate used in SVM, the equivalent carrier based techniques have been developed. CBSVM is appropriate for inverters with more than five levels, where the computational overhead for conventional SVM is exceeding due to many output states. CBSVM is derived from the addition of a common offset voltage to the three phase references it will center the active space-vectors in the switching period, and hence match carrier modulation to get optimized space vector modulation [10].

Generally, carrier based PWM of a multilevel inverter can only select four switching states at most, but SVM can select more. Selection of switching states has more freedom in multilevel SVM than in multilevel carrier based PWM. In order to solve that problem, multilevel SVM can also be decomposed into several two level carrier based PWM cells. This method effectively increases the number of switching in a multilevel SVM scheme greater than in a conventional PWM scheme, but the additional switching is mainly added in the area the modulated wave is steep, where the output wave may be distorted most seriously, so it is more effective to improve the output voltage by using a multilevel SVM scheme than by increasing frequency of carrier waves directly. Furthermore, more freedom of switching selection of multilevel SVM is also propitious to power balance of H-bridge cells in a cascaded multilevel inverter. The optimal switching sequence can be achieved by using a proper offset voltage.

The appropriate offset voltage for v_{off}' multilevel operation can be expressed by the following equations so that the comparison between multicarriers and references generates the optimized switching sequence.

$$V_{off} = -\frac{\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)}{2}\sqrt{a^2+b^2} \qquad (1)$$

$$V_k' = (V_k + V_{off} + V_{dc}) \bmod \left(\frac{2V_{dc}}{N-1}\right),\ k = a,b,c \qquad (2)$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a',V_b',V_c')+\min(V_a',V_b',V_c')}{2} \qquad (3)$$

where v_{dc} is 1 p.u. Addition of a proper offset voltage to phase voltage references v_a, v_b, or v_c generates modified references, and CBSVM signals for each phase leg switches can be generated throughout the comparison between the respective modified references and phase disposition carriers.

3. PROPOSED HYBRID CARRIER BASED SPACE VECTOR MODULATION

The proposed hybrid carrier based space vector modulation is a combination of fundamental frequency PWM and carrier based space vector modulation. The basic principle behind the proposed scheme, the four power devices in each full bridge of a cascaded inverter are operated at two different frequencies, two being commutated at the fundamental frequency of the output, while the other two power devices are pulse width modulated at CBSVM. This arrangement causes the problem of differential switching losses among the switches. This technique is optimized with a sequential signal and the resultant hybrid CBSVM pulses overcome this problem. In this modulation strategy, three base PWM signals are required for each converter in a cascaded multilevel inverter. A sequential signal (A) is a square signal with 50% duty ratio and it has half of the fundamental frequency. This signal makes every power switch operating at CBSVM and low frequency PWM sequentially.

Fundamental frequency PWM (B) is a square wave signal synchronized with the modulation waveform, and it is defined as B=1 during the positive half cycle of the modulation signal, and as B=0 during the negative half cycle of the modulation signal. CBSVM is based on the comparison of a modified sinusoidal reference signal ($v_k + v_{off}\ v_{off}'$) with each carrier to determine the voltage level that the inverter should switch to. In this carrier based N level PWM operation consists of N-1 different carriers, where all carriers are in phase. A sequential switching signal and low frequency PWM signals are the same for all full bridge converter cells. The base PWM signals (A, B, C and D) for a hybrid PWM controller are shown in Fig. 2.

A hybrid PWM controller is implemented using a simple combinational logic, and hence, it can be processed very quickly. The functions of the combinational logic for a five-level hybrid PWM are expressed as

$$S1 = A\,B\,C + \overline{A}\,B \qquad S1' = A\,B\,D + \overline{A}\,B$$
$$S2 = \overline{A}\,B\,C + \overline{A}\,\overline{B} \qquad S2' = \overline{A}\,B\,D + \overline{A}\,\overline{B}$$
and
$$S3 = \overline{A}\,\overline{B}\,C + A\,\overline{B} \qquad S3' = \overline{A}\,\overline{B}\,D + A\,\overline{B}$$
$$S4 = \overline{A}\,B\,C + A\,B \qquad S4' = \overline{A}\,B\,D + A\,B$$

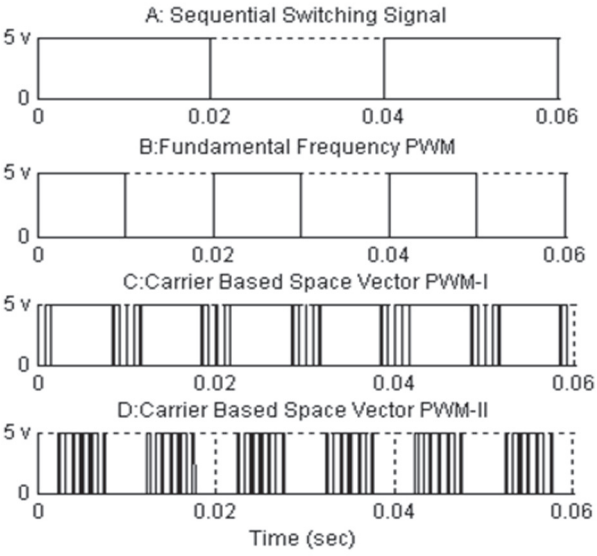


Fig. 2. Base PWM signals for five-level hybrid carrier-based space vector modulation

In Fig. 3, it is shown that each gate signal is composed of both low frequency PWM and CBSVM signals. If sequential switching signal A=1, S1 and S2 in converter 1 and S1′ and S2′ in converter 2 are operated with CBSVM while S3 and S4 in converter 1 and S3′, S4′in converter 2 are operated at fundamental frequency. If sequential switching signal A=0, S1 and S2 in converter 1 and S1′ and S2′ in converter 2 are operated at fundamental frequency while S3 and S4 in converter 1 and S3′, S4′in converter 2 are operated with CBSVM. Since A is a sequential signal, the average switching frequency amongst the four switches and power loss are equalized. Thermal stress of power switches in each inverter bridge is also inherently equalized with this modulation.

For completeness, the generalized formulation that suits for an N-level inverter and for any number of switching transitions is presented. The proposed algorithm for an N-level inverter is as follows:

1. Obtain the number of inverter cells K=N-1/2.
2. Modify the peak amplitude of phase reference voltages v_a, v_b and $v_c$based on modulation index $M=A_m/K\ A_c$, where Am is the amplitude of a modulation signal and Ac is the amplitude of a carrier signal.
3. Identify the instantaneous values of three phase reference voltages v_a, v_b, and v_c and determine the values of v_{off} and v_{off}'.
4. A modified sinusoidal reference signal is obtained by $v_k' = v_k + v_{off} + v_{off}'$.
5. Comparison of a modified sinusoidal modulating signal with each phase disposition carrier signal separately to generate a K number of carrier based space vector modulation signals.

6) A common sequential signal and fundamental frequency PWM signals for each phase are obtained in synchronization with a modulating signal.

7) An independent hybrid controller (combinational logic circuit) is used to mix low frequency PWM and the corresponding carrier based SVM for each inverter cell.

$$Sx1 = A\ B\ X + \overline{A}\ B;\ Sx2 = \overline{A}\ B\ X + \overline{A}\ \overline{B};$$
$$Sx3 = \overline{A}\ \overline{B}\ X + A\ \overline{B};\ Sx4 = \overline{A}\ B\ X + A\ B$$

8) Similarly, hybrid PWM pulses are developed for all cells in any level cascaded inverter. Totally 4K gate pulses per phase are developed to operate an N-level cascaded multilevel inverter.

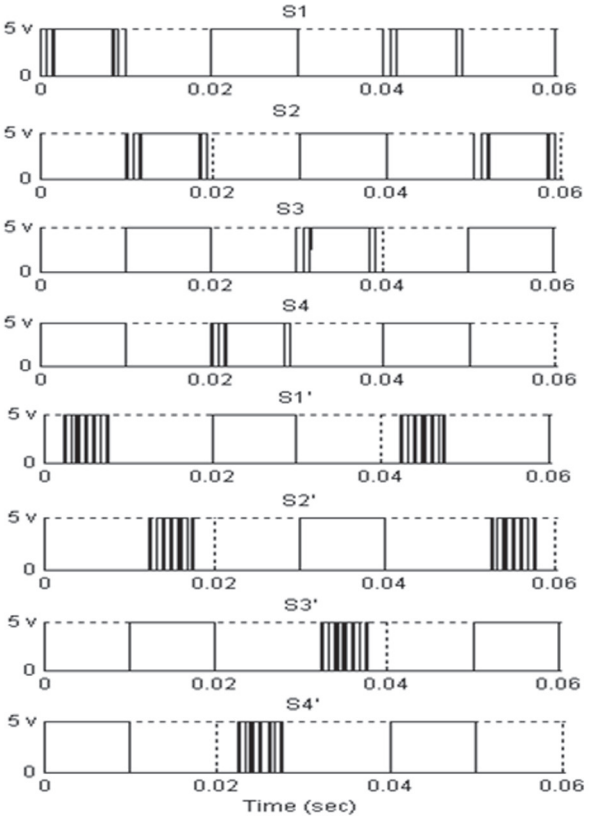


Fig.3. Hybrid carrier based space vector modulation signals for a five-level cascaded multilevel inverter

4. POWER LOSS MINIMIZING CONTROL AND ANALYSIS

Power loss optimization is achieved in this paper by the proposed modulation technique in which

1. Proper offset voltage v_{off} and v_{off}' are developed and added to the phase reference voltages to get an optimized CBSVM.
2. CBSVM is combined with fundamental frequency PWM using a hybrid PWM control algorithm, so that the number of commutations of semiconductors per unit time in the operation of multilevel inverters is reduced.
3. An optimized sequential signal is added to hybrid PWM signals to balance the power loss among the power devices. Each power device present in the cascaded inverter operates with fundamental frequency PWM (two commutations per cycle) and CBSVM (the number of commutations proportional to switching frequency) for one fundamental period. So the number of semiconductor switching is half of the conventional space vector modulation. This technique is also designed to get the optimum number of switching events based on the modulation index and the phase angle between voltage and current fundamentals.

The losses in power converters can be classified as: conduction loss, switching loss, snubber loss, and off-state loss. Since the leakage current during the off state of the device is negligibly small, the power loss during the off state can be neglected. Snubber losses can be important in some kinds of power devices, such as gate turn-off thyristors [11]. Thus, only conduction and switching losses are considered in this paper. New high power devices can switch faster. Since switching losses are directly related to the switching frequency, these losses are usually greatest in PWM power converters.

MATLAB-Simulink model of a five-level inverter has been developed to study the power loss. The carrier frequency f_s is 2 kHz and each converter cell is connected to a 200 V DC supply. The IGBTs selected are FF150R12KT3G, in which their maximum ratings are a forward current of 150 A and a direct voltage of 600 V. The semiconductor power losses can be estimated from the curves ($V_{sat}(\theta)$ x $I_1(\theta)$) and ($E(\theta)$ x $I_1(\theta)$), presented in the datasheet of each device, where : V_{sat} is the on-state saturation voltage ($V_{ce}(\theta)$ for the IGBT and $V_F(\theta)$ for the diode); $E(\theta)$represent energy losses in one commutation ($E_{on}(\theta)$ if it is a turn-on commutation, $E_{off}(\theta)$ if it is a turn-off commutation and $E_{rec}(\theta)$ if it is a diode reverse recovery process). These curves are used in a Matlab script developed to determine the power losses. Mathematical models are found using points extracted from datasheets of each semiconductor device. Mathematical models obtained for the IGBT module FF150R12KT3G are given by

$$V_F = 1.2\, e^{0.002\, I_1(\theta)} - 0.7258\, e^{-0.0475\, I_1(\theta)}$$

$$V_{ce} = 1.15\, e^{0.0026\, I_1(\theta)} - 0.6654\, e^{-0.044\, I_1(\theta)}$$

$$E_{rec} = 0.01806\, e^{-0.000412\, I_1(\theta)} - 0.0157\, e^{-0.00736\, I_1(\theta)}$$

$$E_{on} = 0.0051\, e^{0.0064\, I_1(\theta)} - 0.0037\, e^{-0.00811\, I_1(\theta)}$$

$$E_{off} = 0.0643\, e^{0.00121\, I_1(\theta)} - 0.0647\, e^{-0.00107\, I_1(\theta)}$$

$$I_1(\theta) = M \bullet I_{max} \sin(\theta - \phi)$$

where $I_1(\theta)$is the load current, M is the modulation index and φ is the load displacement angle.

Conduction and switching power losses are calculated based on mathematical models for each semiconductor device of the inverter. The sum of all results is computed to obtain the total power losses. The total power losses are the sum of conduction and switching losses.

$$P_{Total} = P_{cond} + P_{sw}$$

Switching losses are generated during the turn-on and turn-off switching processes of power devices. In such processes, the voltages and currents can take significant values simultaneously. Therefore, their instantaneous power can reach high values. Fortunately, these processes only last for short periods, although they are repeated several times within a second. For this reason, they are directly related to the switching frequency. Switching losses are obtained by identifying every turn-on and turn-off instant during one reference period.

$$P_{sw} = \frac{1}{T} \sum (E_{on} + E_{off} + E_{rec})$$

Conduction power losses are those that occur while a semiconductor device is conducting current. Conduction losses of transistors are obtained from linearization of the static characteristics of power switches. The calculation of conduction power losses are given by

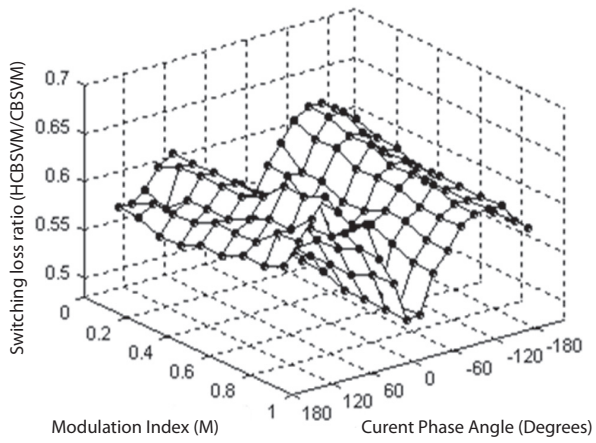
$$P_{cond\_IGBT} = \frac{1}{2\pi} \int_0^{2\pi} V_{ce}(\theta) \bullet I_1(\theta) \bullet V_{cmd}(\theta)\, d\theta$$

$$P_{cond\_D} = \frac{1}{2\pi} \int_0^{2\pi} V_F(\theta) \bullet I_1(\theta) \bullet V_{cmd}(\theta)\, d\theta$$

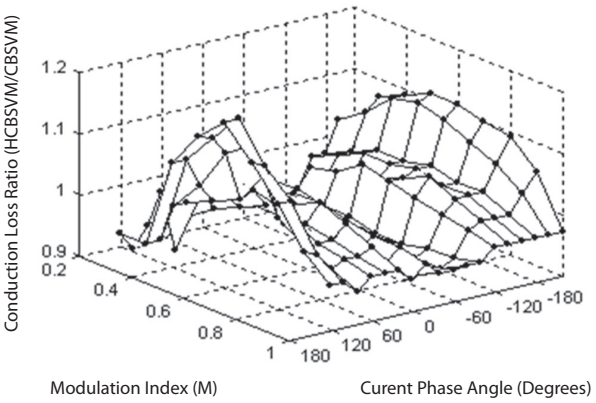
$$P_{cond} = P_{cond\_IGBT} + P_{cond\_D}$$

where $V_{cmd}(\theta)$ is the PWM signal of the IGBT

For a full range of a modulation index and the relative angle of the output currents, Fig.4 (c) shows the ratio of total power losses for a five-level inverter with the proposed modulation strategy versus the conventional CBSVM technique. Note that the surface is always below one, which means that power losses are significantly smaller for the proposed method. The mean value of the loss ratio is found to be approximately 0.73, which implies the power loss reduction of about 27%. The best case is produced for a unity power factor and a modulation index of one. In a practical high power system, switching losses are higher than conduction losses. Therefore, saving switching losses becomes important for improvement of the system efficiency.



(a)



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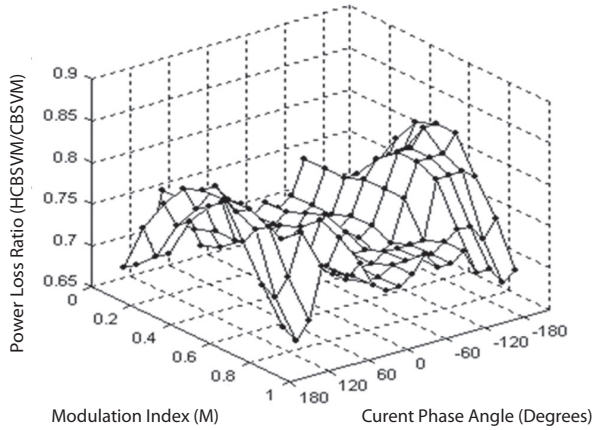


(c)

Fig.4. Ratio of the losses of hybrid carrier based space vector modulation and conventional CBSVM fed five-level cascaded inverters.
(a) Switching Losses.
(b) Conduction Losses.
(c) Total Power Loss.

5. RESULTS AND DISCUSSION

5.1. SIMULATION RESULTS

In order to verify that the proposed modulation can be practically implemented in a cascaded inverter, simulations were performed by using MATLAB/Simulink. It also helps to confirm the PWM switching strategy which can be implemented in a digital signal processor (DSP) and a complex programmable logic device (CPLD). The performance index, namely total harmonic distortion (THD), is chosen for quantification of the proposed hybrid CBSVM. The total harmonic distortion of a signal is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The THD is calculated using (4) and plotted in Fig.5 and it is taken into account up to the 50th order of harmonics. The low pass filter and the nature of the highly inductive load will take care of the higher order of harmonics. It is obviously found that the proposed PWM offers a lower THD compared to the conventional one, thus the superiority. Furthermore, it is also noticed that the higher value of the modulation index (M) the lower the value of THD and for the increased frequency ratio.

$$THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^2}}{V_1} \times 100 \qquad (4)$$

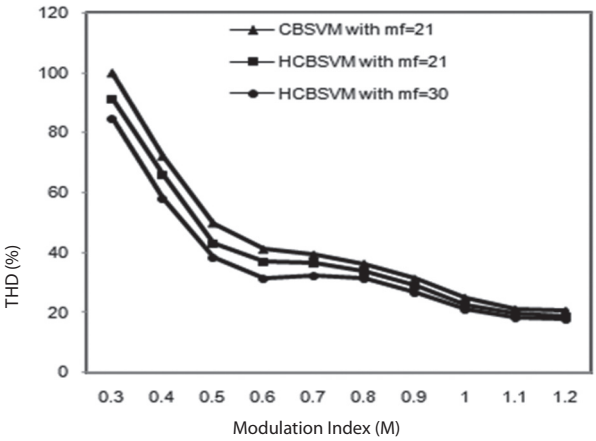
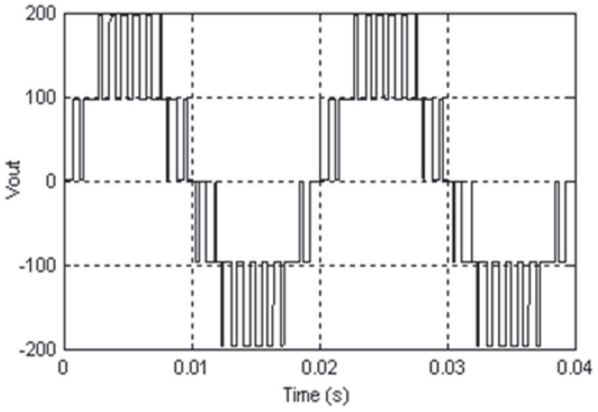
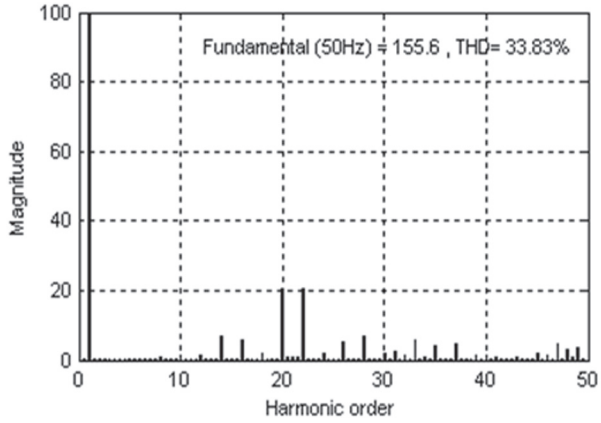


Fig. 5. THD comparision of a five-level cascaded inverter with the proposed modulation

The inverter is operated with the proposed modulation in a linear modulation range and the corresponding voltage waveform with the FFT analysis is shown in Fig.7. It can be seen that all the lower order harmonics are absent and the fundamental is controlled at the predefined value. It is interesting to note that the next significant harmonic will be the 35th for a frequency ratio of 21. The significant harmonics are 35, 39, 41, and 45, which are of high frequency, with the rms values under 11% of the fundamental term. The compared conventional PWM operation is shown in Fig.6, the FFT spectrum of the proposed inverter output voltage gives superiority.

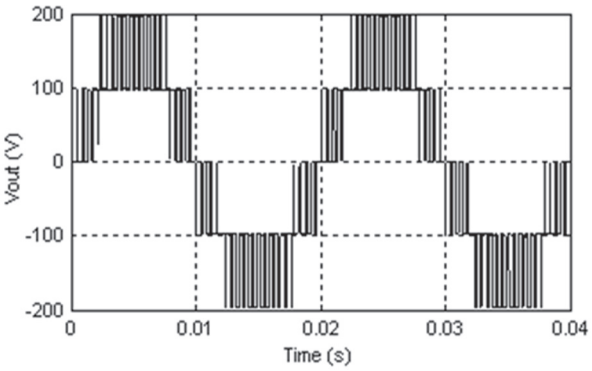


(a)



(b)

Fig. 6. Simulation results of conventional CBSVM operation in a linear modulation region (M=0.8, fo =50 Hz, fc =1050 Hz)
(a) Output phase voltage waveform.
(b) Spectrum of the output voltage waveform.



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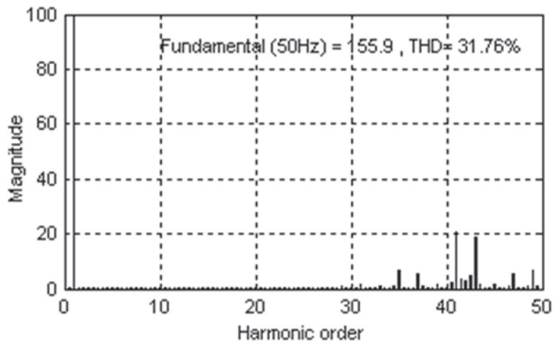
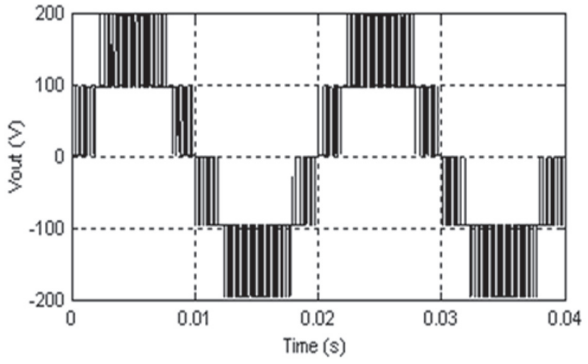
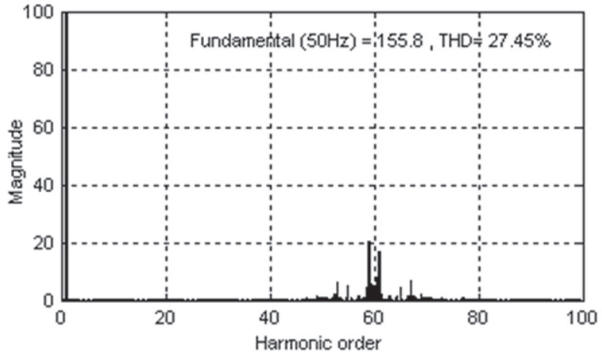


(b)

Fig. 7. Simulation results of hybrid CBSVM operation in a linear modulation region (M=0.8, fo =50 Hz, fc =1050 Hz)
(a) Output phase voltage waveform.
(b) Spectrum of the output voltage waveform.



(a)



(b)

Fig. 8. Simulation results of hybrid CBSVM operation in a linear modulation region (M=0.8, fo =50 Hz, fc =1500 Hz)
(a) Output phase voltage waveform.
(b) Spectrum of the output voltage waveform.

5.2. EXPERIMENTAL RESULTS

A functional block diagram of hybrid modulation controller implementation for a five-level cascaded inverter is shown in Fig.9. The inverter is made with eight insulated gate bipolar transistor (IGBT) switches with internal anti-parallel diodes. Texas instruments TMS320F2407 digital signal processor (DSP) is chosen for base PWM generation as it has dedicated PWM units that utilize high speed counters/timers with accompanying compare registers. The structure of CBSVM is very simple and it requires only a few mathematical operations in order to provide modulation signals. The PWM unit is initialized by defining parameters such as symmetric carrier, switching frequency, PWM polarity, and to modulation signals for compare registers. The appropriate offset components are calculated based on phase voltage references. After adding zero sequence signals to fundamental signals, modulation signals are ready to be loaded into compare registers of a PWM unit. A sequential signal is also generated to operate each IGBT with fundamental frequency PWM and CBSVM sequentially to equalize power losses, heating among the devices.

The proposed hybrid modulation algorithm is implemented using Xilinx CPLD XC95108 IC. A CPLD controller combines fundamental frequency PWM, sequential signal and CBSVM to generate hybrid CBSVM pulses. XC95108 IC is used to develop a control algorithm which is suited for this application that has features of a better response for high frequency input signals, narrow pulse width pulses and no jitter of the delay in the circuit. A switching dead time of 600 ns is introduced in the CPLD hardware. Optically coupled isolators MCT2E are used to provide an electrical isolation between the Xilinx CPLD controller board and the power circuit. Four high voltage high speed IGBT drivers (IR2112) are used to provide proper and conditioned gate signals to power switches.

A digital real time oscilloscope (Tektronix TPS2024) is used to display and capture the output waveforms and with the feature of the fast Fourier transform (FFT), the spectrum of the output voltage is obtained for different operating points as discussed hereafter. Selected experimental results for a five-level inverter were obtained and validated the simulation results.

Specifically, Fig.10 (a) shows the line to a neutral voltage waveform of the proposed five-level CBSVM operation in a standard modulation and the associated spectrum is presented in Fig.10 (b). It is confirmed that the harmonic cancellation up to sidebands around double the carrier frequency is achieved in the voltage waveform and the first significant harmonic is the 17th, as predicted. The over-modulation operation for the proposed method is also experimentally verified and results are presented in Fig.11. As expected, the spectrum shows that a lower order harmonic (5th) is introduced with a lower magnitude in addition to side-band harmonics. This shows that the hybrid PWM modulator is capable of taking the system from a linear mode to an over-modulation mode smoothly.

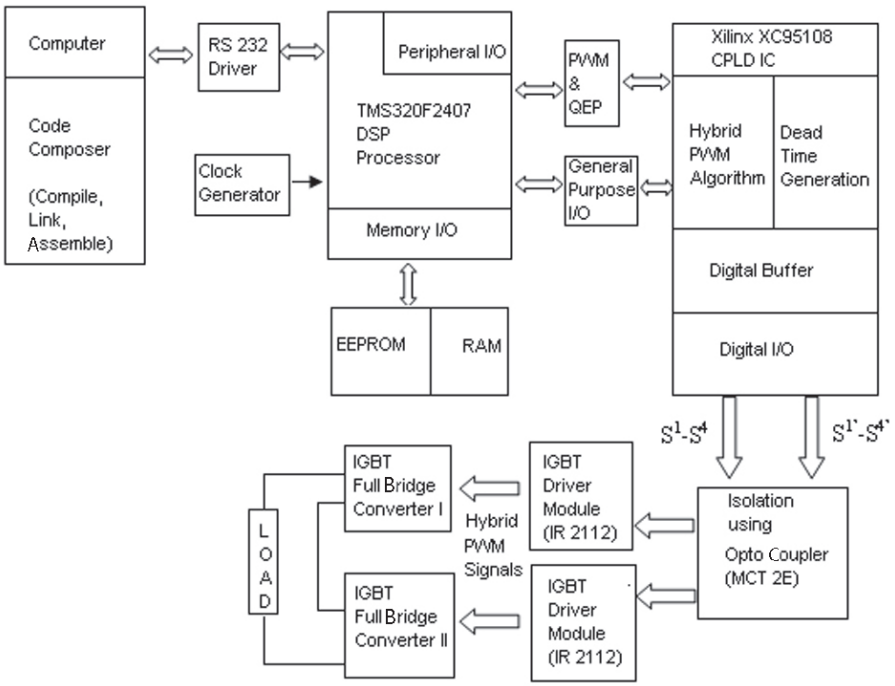
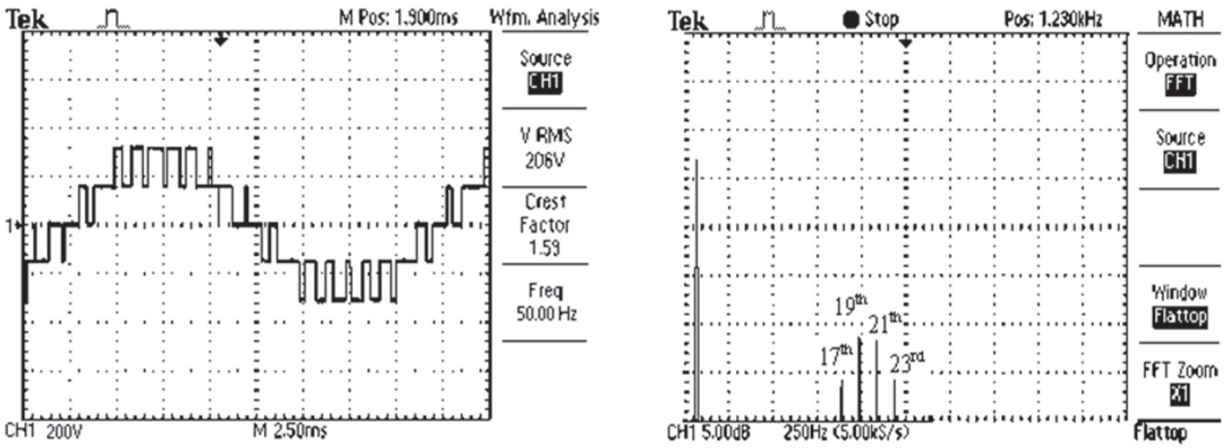
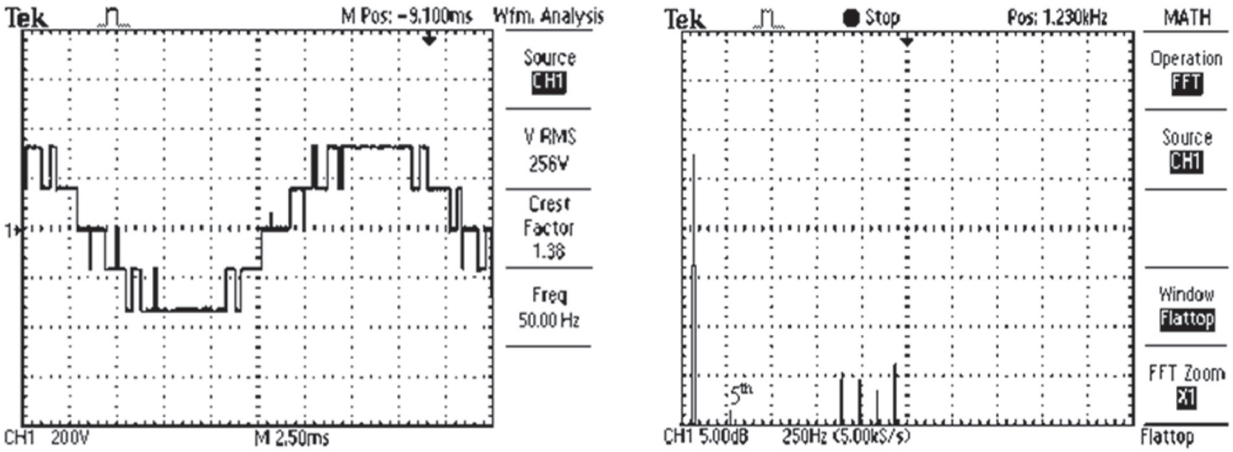


Fig. 9. Functional block diagram of hybrid CBSVM implementation (one phase)



(a) (b)

Fig.10. Experimental results of hybrid CBSVM operation in linear modulation (a) phase voltage waveform. (b) Spectrum of the phase voltage waveform



(a) (b)

Fig. 11. Experimental results of the hybrid CBSVM in over-modulation range. (a) Output voltage waveform. (b) Spectrum of the output voltage waveform.

6. CONCLUSION

This paper proposed an energy efficient hybrid carrier based space vector modulation for a cascaded multilevel inverter. The hybrid PWM control algorithm is developed to derive the features of fundamental frequency PWM and carrier based space vector modulation for an inverter operation, with the same physical structure. Compared to conventional CBSVM, a reduced number of commutations of semiconductors per unit time is obtained while achieving the same fundamental voltage tracking and it offers 27% of power loss saving. Better harmonic performance of the proposed PWM strategy compared to its CBSVM in the entire range of the modulation index is shown. The proposed technique can be applied easily to higher level inverters through the generalization process. The presented strategy and its results represent an illustration of the advantages that can be obtained by applying power loss minimizing control to multilevel inverters.

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