ISSN 0005–1144
ATKAAF 42(1–2), 37–44 (2001)

Rafael Ramos, Domingo Biel, Francesc Guinjoan, Enric Fossas

Master-Slave Sliding-Mode Control Design in Parallel-Connected Inverters

UDK 621.311.68
IFAC IA 5.5.4;4.7.1

Original scientific paper

This work presents the design of a master-slave sliding-mode control scheme for a modular inverter system composed of *N* parallel-connected Buck-based single inverters. AC output voltage regulation and balanced current-sharing among the single inverters is achieved by means of a set of switching surfaces and the corresponding sliding control laws. On the other hand, a set of design restrictions is established in terms of inverter parameters and AC output signal amplitude and frequency, this facilitating the subsequent design procedure. Simulation and experimental results for both resistive and nonlinear loads are provided to illustrate the application of the method.

Key words: buck inverter, master-slave, parallel modules, sliding-mode control

1. INTRODUCTION

Power management flexibility and reliability of power inverter systems can be improved when a modular structure resulting from the paralleling of single inverter modules is adopted. On one hand, the modular structure enables the total power increase of the power inverter system by increasing the number of inverter modules. Furthermore, for a fixed power capability, device stresses can be reduced by adding inverter modules, since the power density handled by each module is reduced. On the other hand, redundant modules can be included, this leading to fault-tolerant modular structures in the case of inverter module failure. Accordingly, the power inverter system reliability is improved [8–10]. However, parallel inverter modules are usually non-identical due to the finite tolerances in the power stage parameters, this resulting in an unbalanced current-sharing among the modules. Consequently, one or more modules may handle an excessive load current.

In order to prevent this problem, the Master-Slave control technique is one of the several control policies ensuring both the output voltage amplitude regulation and the desired current distribution among the power inverter modules [8]. This technique is based on the principle of that one of the inverter modules is constrained to behave as a sinusoidal voltage source (Master inverter), while the other modules behave as balanced current sources (Slave inverters). These requirements can be fulfilled on one hand, by means of the design of a voltage control loop for the master inverter ensuring the tracking of an external sinusoidal reference signal. On the other hand, the balanced current sources behavior is performed by designing a current-control loop for each of the slave inverters, where the inductor current of the Master inverter acts as a current reference. This control policy has been generally applied to PWM-based parallel inverters [9]. In this case, the design of all the aforementioned control loops is based on a linearized power stage model, this leading to output waveforms sensitive to power stage parameter variations, such as the output load. Alternatively to PWM control strategies, and based on their robustness properties in front of parameter variations, sliding-mode control techniques have been applied to the control loop design of several power systems such as single switching DC-DC converters [4, 6], single inverters [2, 7] and to a central-limit control scheme for parallel-connected switching DC-DC power supplies [10].

The work here reported presents the design of a master-slave sliding-mode control scheme for an inverter system of *N* buck-based parallel-connected inverters. The paper is organized as follows: based on the master-slave control approach, section two introduces a set of switching surfaces and their corresponding sliding control laws leading to the desired steady-state behavior in the sense of output voltage regulation and balanced current sharing. Subsequently, in section three, the obtention of the overall inverter system sliding domain is derived in terms of the output filter Bode diagrams of each converter and the output signal parameters (ampli-

tude and frequency), this facilitating the subsequent design. Experimental results obtained in an electronic prototype of two parallel-connected inverters loaded with a nonlinear load are shown in section four. Finally, the last section summarizes the conclusions of the work.

2. INVERTER MASTER-SLAVE SLIDING CONTROL

Figure 1 shows a power inverter system composed by N parallel-connected Buck converters.

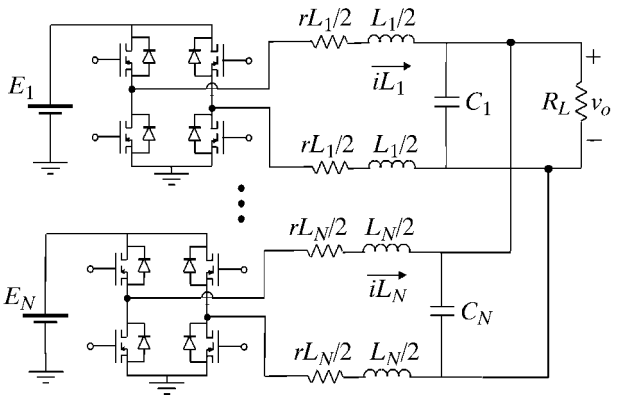

Fig. 1 Electrical scheme of N parallel-connected Buck power converters

The dynamical behavior of this system can be represented by the following state equation:

$$\begin{cases} \dfrac{\mathrm{d}iL_1}{\mathrm{d}t} = -\dfrac{rL_1}{L_1}\cdot iL_1 - \dfrac{1}{L_1}\cdot v_o + \dfrac{E_1}{L_1}\cdot u_1 \\ \dfrac{\mathrm{d}iL_2}{\mathrm{d}t} = -\dfrac{rL_2}{L_2}\cdot iL_2 - \dfrac{1}{L_2}\cdot v_o + \dfrac{E_2}{L_2}\cdot u_2 \\ \quad\vdots \\ \dfrac{\mathrm{d}iL_N}{\mathrm{d}t} = -\dfrac{rL_N}{L_N}\cdot iL_N - \dfrac{1}{L_N}\cdot v_o + \dfrac{E_N}{L_N}\cdot u_N \\ \dfrac{\mathrm{d}v_o}{\mathrm{d}t} = \dfrac{1}{\sum_{i=1}^{N} C_i}\cdot iL_1 + \dfrac{1}{\sum_{i=1}^{N} C_i}\cdot iL_2 + \ldots \\ \qquad \ldots + \dfrac{1}{\sum_{i=1}^{N} C_i}\cdot iL_N - \dfrac{1}{\left(\sum_{i=1}^{N} C_i\right) R_L}\cdot v_o \end{cases} \tag{1}$$

where u_i designates the control input of ith-converter. The control variable u_i takes values in the discrete set $u_i \in \{1, -1\}$ corresponding to a full bridge switch, this ensuring the bipolarity of the AC output voltage.

The main goal of the control policy is to provide both AC output voltage regulation and balanced current-sharing among the inverter modules. In this work the sliding mode control technique has been adopted to achieve these control features due to its robustness in from of perturbations, namely variations of the input voltage and/or in the load [2, 7].

As far as the voltage regulation is concerned, the following switching surface proposed by Carpita et. al. [7] has been applied due to its independence to the converter parameters:

$$\sigma = \alpha\cdot\left(V_{\mathrm{ref}}(t) - v_o\right) + \left(\frac{\mathrm{d}V_{\mathrm{ref}}(t)}{\mathrm{d}t} - \frac{\mathrm{d}v_o}{\mathrm{d}t}\right) = \alpha\cdot e(t) + \frac{\mathrm{d}e(t)}{\mathrm{d}t}$$

$$\text{where} \quad V_{\mathrm{ref}}(t) = A\cdot\sin(2\pi ft)\,. \tag{2}$$

This switching surface will be assigned to one of the Buck inverters in order to track the AC voltage reference signal.

The balanced current-sharing among the inverter modules can be performed by means of a Master--Slave control algorithm, in the sense of that the inductor current of the voltage-controlled converter (acting as a Master) is considered as the inductor current reference for the other inverter modules (Slaves).

In terms of sliding mode control the following switching surfaces can be proposed to achieve the previous requirements:

$$\begin{aligned} \sigma_1(t) &= \frac{\mathrm{d}e(t)}{\mathrm{d}t} + \alpha\cdot e(t) \quad \text{(Master)} \\ \sigma_2(t) &= iL_1(t) - iL_2(t) \quad \text{(Slave)} \\ &\vdots \\ \sigma_N(t) &= iL_1(t) - iL_N(t) \quad \text{(Slave)}. \end{aligned} \tag{3}$$

Therefore, this sliding mode control considers a voltage loop (Master module) and N–1 current loops (Slave modules).

It can be pointed out that, from the equations (2) and (3), proper control actions lead to the desired steady state sliding motion, that is:

$$e(t) \to 0 \Rightarrow v_o \to V_{ref}(t)$$
$$\text{and}$$
$$iL_1(t) = iL_2(t) = \cdots = iL_N(t).$$

These control actions can be obtained from the Lyapunov stability criteria by imposing $\dfrac{\mathrm{d}\sigma_i^2}{\mathrm{d}t} < 0$ ($i = 1 \ldots N$), this leading to:

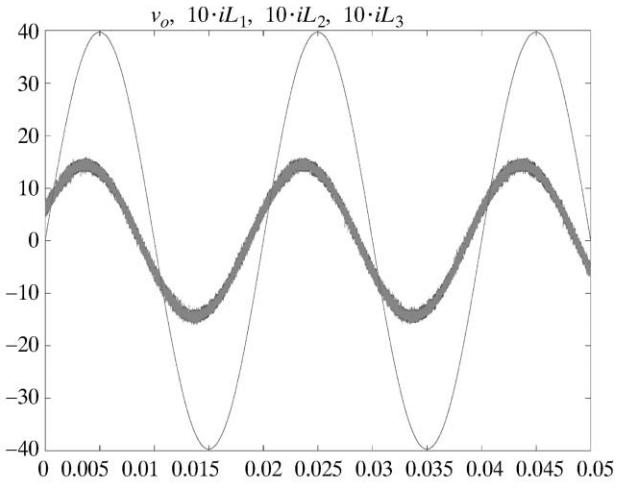

Fig. 2 Simulation results of a Master-Slave three parallel-connected Buck power converters

$$u_1 = \begin{cases} +1 & \text{when} \quad \sigma_1 > 0 \\ -1 & \text{when} \quad \sigma_1 < 0 \end{cases} \quad \text{for the master module}$$

$$u_j = \begin{cases} +1 & \text{when} \quad \sigma_j > 0 \\ -1 & \text{when} \quad \sigma_j < 0 \end{cases} \quad \text{for the slave modules.} \tag{4}$$

The previous control policy has been simulated with MATLAB-SIMULINK software in the case of three parallel-connected Buck converters with the following mismatched parameters $E_1 = E_2 = E_3 = 50$ V, $L_1 = 1$ mH, $L_2 = 500$ μH, $L_3 = 750$ μH, $C_1 = 60$ μF, $C_2 = 20$ μF, $C_3 = 60$ μF, $rL_1 = rL_2 = rL_3 = 0$ Ω, $R_L = 10$ Ω, $\alpha = 5000$ when a desired output voltage is fixed to $v_o(t) = 40 \sin(2\pi 50t)$. Figure 2 shows the output voltage and the inductor currents obtained in the simulation.

3 DESIGN RESTRICTIONS

The desired steady-state assume a sliding motion over all the switching surfaces defined in (3). Considering a single switching surface σ_i, and the corresponding control law u_i, and accounting for sliding mode control principles, the sliding motion over σ_i is ensured when the state trajectories of the overall system intersect this switching surface into a region, defined as the sliding domain of σ_i [4, 5]. This sliding domain can be determined from the obtention of the corresponding equivalent control, $u_{eq\,i}$ which can be derived by applying the invariance condition [4, 5], i.e:

$$\begin{cases} \sigma_i = 0 \\ \left(\dfrac{\mathrm{d}\sigma_i}{\mathrm{d}t} \right)_{u_i = u_{eq_i}} = 0 \end{cases} \qquad (i = 1 \ldots N) \tag{5}$$

from the later, the steady state equivalent control is given by:

$$u_{eq_i} = \frac{L_i}{N \cdot E_i} \cdot \left[V_{\mathrm{ref}} \left(\frac{rL_i}{R_L L_i C_T} + \frac{N}{L_i C_T} \right) + \right.$$

$$\left. + \frac{\mathrm{d}V_{\mathrm{ref}}}{\mathrm{d}t} \left(\frac{rL_i}{L_i} + \frac{1}{R_L C_T} \right) + \frac{\mathrm{d}^2 V_{ref}}{\mathrm{d}t^2} \right] \tag{6}$$

where $C_T = \sum_{i=1}^{N} C_i$.

The sliding domain can be obtained by imposing $-1 < u_{eqi} < 1$, this leading to:

$$\frac{A}{E_i} < |\gamma_i(\omega)| \tag{7}$$

where

$$|\gamma_i(\omega)| = \left\{ \left(\frac{L_i \omega}{N R_L} \right)^2 + \left(\frac{C_T L_i \omega^2}{N} - 1 \right) + \right.$$

$$\left. + \frac{rL_i}{N} \cdot \left[\frac{C_T^2 rL_i \omega^2}{N} + \frac{rL_i}{N R_L^2} + \frac{2}{R_L} \right] \right\}^{-\frac{1}{2}} . \tag{8}$$

This expression corresponds to the frequency response of the *i*th-converter output filter taking into account the parallel connection, which transfer function is given by:

$$\gamma_i(s) = \frac{\dfrac{N}{L_i C_T}}{s^2 + \left(\dfrac{rL_i R_L C_T + L_i}{R_L L_i C_T} \right) \cdot s + \dfrac{rL_i}{R_L L_i C_T} + \dfrac{N}{L_i C_T}} \cdot \tag{9}$$

As a result, the sliding domain of σ_i can be expressed as a function of this frequency response and the output signal parameters (amplitude A and frequency ω).

Therefore the sliding regime over σ_i is ensured for the values of the output amplitude-input voltage ratio A/E_i lying below the plot of the output filter response $\gamma_i(\omega)$.

As the sliding motion has to be ensured over all the switching surfaces this previous analysis must be performed for all of them. As a result, the sliding domain of the overall system correspond to the intersection of the individual sliding domains, this leading to the following condition:

$$A < E_i \cdot |\gamma_i(\omega)| \quad \forall i \tag{10}$$

Figure 3 shows the frequency responses $\gamma_i(\omega)$ for a parallel-connected inverter system composed by three-Buck converters with the parameters defined

in section 2 and the single frequency responses when no parallel connection is adopted. In this Figure the dashed area displays the set of values of A/E as function of ω where the sliding motion is guaranteed.

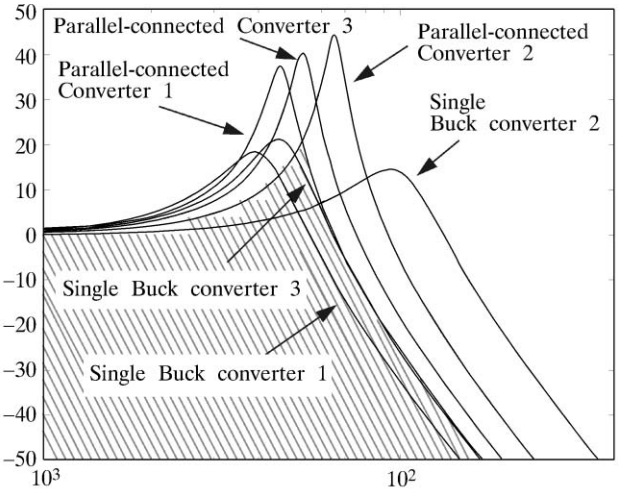

Fig. 3 Values of A/E (dashed area) where the steady-state behavior can be reached in three parallel-connected Buck based inverters

Comparing with the case of a single inverter [1], it can be noted that the paralleling connection modifies the resonant frequency and decreases the damping factor of the frequency response of the *i*th-converter output filter. Consequently these considerations have to be taken into account in the design procedure. Explicitly, as far as load variations are concerned, when the load decreases the damping factor of the over all system decreases too. For this reason, the design has to take into account the minimum load value for which a sinusoidal output signal is desired.

The sliding domain analysis is not restricted to resistive loads and can be generalized to nonlinear loads, leading to a sliding domain given by:

$$\frac{L_i C_T}{N \cdot E_i} \cdot \left| \frac{1}{C_T} \left(i_z \frac{rL_i}{L_i} + \frac{\mathrm{d}i_z}{\mathrm{d}t} \right) + \frac{N \cdot V_{\mathrm{ref}}}{C_T L_i} + \right.$$

$$\left. + \frac{rL_i}{L_i} \cdot \frac{\mathrm{d}V_{ref}}{\mathrm{d}t} + \frac{\mathrm{d}^2 V_{\mathrm{ref}}}{\mathrm{d}t^2} \right| < 1$$

where i_z is the current flowing in the nonlinear load. In this case the parallel system trajectory will escape from the sliding surface when the load has current discontinuities. Consequently the control policy has to be designed in order to recover the desired sliding motion.

On the other hand, in the case of reactive loads the corresponding sliding domain is given by:

$$\frac{A}{E_i} < \frac{N \cdot |Z(j\omega)|}{\left| Z(j\omega) \cdot \left(N - C_T L_i \omega^2 + jC_T r L_i \omega \right) + rL_i + jL_i \omega \right|}$$

where $Z(s)$ is the load impedance. This last expression suggest that when the parallel system feeds a reactive load the design procedure exposed above can also be applied by using the Bode diagram of the output filters loaded with the reactive impedance.

It can be noted that this previous analysis is general and can also be used to study what is the resulting sliding domain when several modules are added or excluded to the modular inverter system.

From (9), as it has been previously mentioned, the damping factor always decreases when the number of parallel-connected modules increases whereas the resonant frequency depends on both the number of converters and the resulting total capacitance C_T. For instance, starting from N^- parallel--connected inverters with a total capacitance C_T^-, where the sliding motion is ensured, the desired steady state behavior can be reached again when several modules are added or removed if

$$C_T{}^+ < \frac{N^+}{N^-} C_T{}^- \tag{11}$$

where N^+ is the final number of connected modules and C_T^+ is the resulting total capacitance.

4. CONTROL SYSTEM IMPLEMENTATION

4.1. Control system circuit description

The inverter control strategy suggested in section 3 has been implemented using a Field Programmable Gate Array. The FPGA-based control scheme and a photo of the PCboard are shown in Figures 4 and 5 respectively.

The prototype has been designed for handling any 84 pins FPGA of the XC4000E series from Xilinx, with PLCC package.

The acquisition system includes two MAX118 A/D converters of 7 analog input channels, 8 bits accuracy, operating at a maximum conversion frequency of 1MS/s. The result of the binary conversion is introduced into the Xilinx FPGA, which has to be properly programmed to carry out all the operations involved in computing the control law.

The 2.5 V voltage reference required for the two A/D converters is delivered by a MX584 voltage reference chip.

On the other hand, the PCboard also includes 16 microswitches acting as a 16 digital inputs and two digital outputs which delivers the control signals of the inverters.

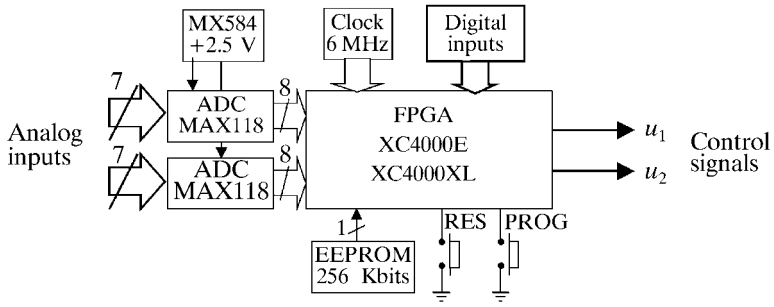

Fig. 4 FPGA-based control scheme

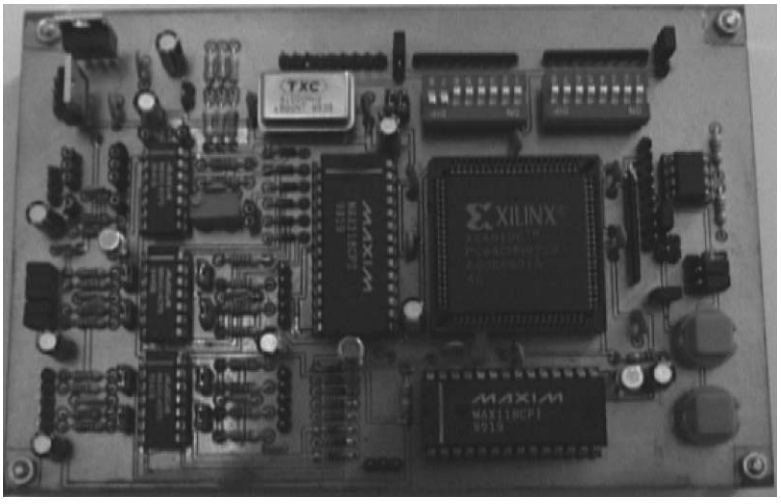

Fig. 5 PCboard of the control system

The FPGA configuration is stored in a 256 Kbits AT17C256 EEPROM memory from Atmel.

Finally, a 6 MHz clock circuit, a reset push button (RES) enabling the FPGA flip-flops initialization, another push button (PROG) allowing a hot reprogrammability of the FPGA, and several operational amplifiers for analog input signals conditioning purposes, have also been implemented.

4.2. Control system circuit operation

Figure 6 shows the main blocks of the FPGA-based control system: the role of the »memory« block is to store the values of the coefficients of the switching surface, the inductor current samples of each converter $i_{L1}(n)$, $i_{L2}(n)$ and the samples of the sum of the voltage error and its derivative $\dot{e}[n]+\alpha e[n]$; the »arithmetic« block is in charge of computing the value of the switching surface corresponding to each converter. Finally, the »sequential« block establishes the signals to control the operation of the A/D converters and the digital circuits embedded into the FPGA.

The »memory« block scheme is depicted in detail in Figure 7. The inputs of this block are on one hand the converters state variables $i_{L1}(n)$, $i_{L2}(n)$, $\dot{e}[n]+\alpha e[n]$ which are sampled with 8 bits accuracy, and on the other hand a set of »digital inputs« corresponding to the values of the coefficients multiplying the state variables, which are introduced with 8 bits accuracy by means of the microswitches.

In addition, the arithmetic block depicted in Figure 8 includes both a c.a.2 multiplier which performs the product between the state variables samples and the coeficients, and a 16 bits accumulator which adds the different products in order to obtain the surface value related to each converter. The switching converters control values are finally computed in the »control signals generator« block according to the sign of each switching surface.

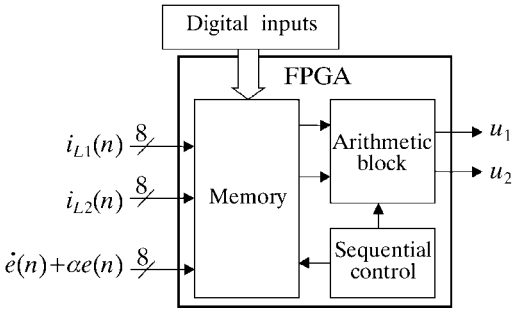

Fig. 6 Main blocks of the FPGA-based control system

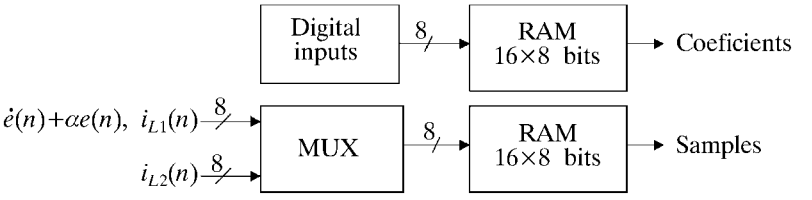

Fig. 7 Memory block scheme

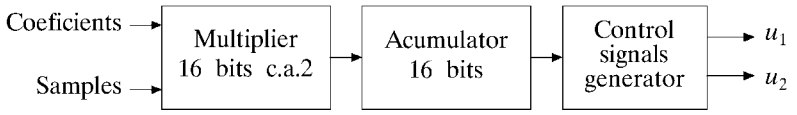

Fig. 8 Arithmetic block

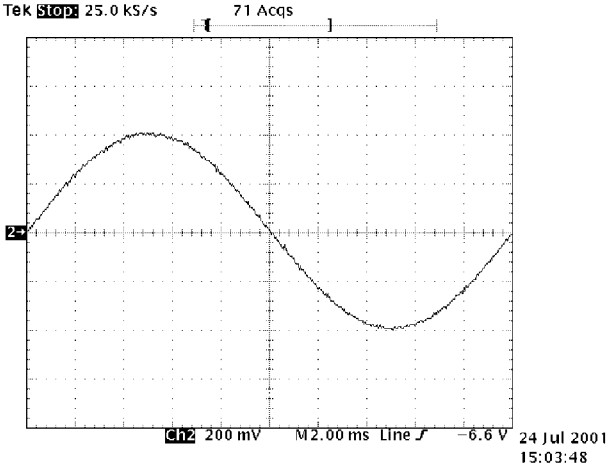

Fig. 9 Measured output voltage of Master-Slave parallel-connected Buck power converters. Scaling factor K = 0.01

Finally, the »sequential control« block generates 24 control signals in order to manage the operation of both the inner blocks of the FPGA and the external A/D converters.

The current implementation presented in this paper is based on the XC4010E-1-PC84 FPGA from the XC4000 Xilinx family. This device includes 10 000 logic gates and 800 flip-flops embedded into 400 CLB (Configurable Logic Block), and 61 IOB (Input/Output Block). The current design has spent 368 CLBs (92 % of the available CLB resources), 44 IOBs (77 % of the available IOB resources) and 75 flip-flops (9 % of the available FF resources). The maximum operating frequency of the design is of 8.59 MHz. The experimental results have been obtained using a 6 MHz clock frequency, this meaning that the time required to compute the master--slave sliding control law is of 2.66 μs.

5. EXPERIMENTAL RESULTS

To experimentally verify the proposed sliding mode control, an electronic prototype has been implemented. The Buck converters parameters are $L_1 = 1.75$ mH, $L_2 = 1.25$ mH, $C_1 = C_2 = 60$ μF, $rL_1 = 133.1$ mΩ and $rL_2 = 107.2$ mΩ. The switching-frequency has been limited by including hysteresis comparators in the control loops [11, 12]. Figures 9

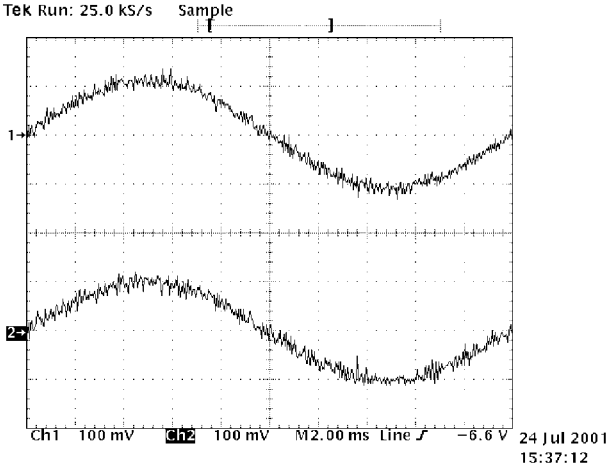

Fig. 10 Measured inductor currents of Master-Slave parallel-conected Buck power converters. Scaling factor K = 50 mV/A

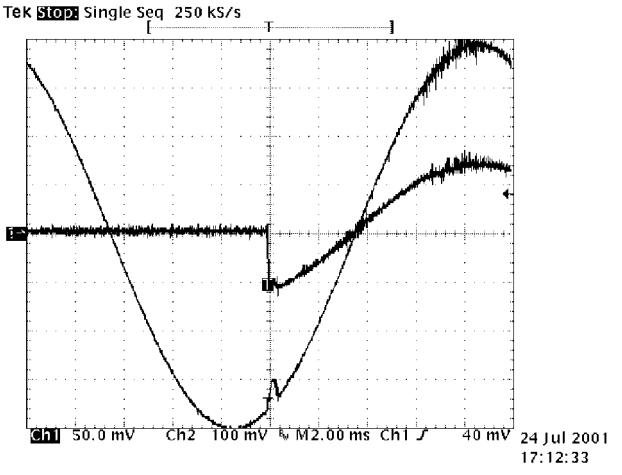

Fig. 11 Measured output voltage and output current of Master-Slave parallel-connected Buck power converters when a step load change has been applied. Voltage scaling factor K = 0.01. Current scaling factor K = 10 mV/A

and 10 show a scaled version of both the measured output voltage and the inductor currents when input voltages are $E_1 = E_2 = 60$ V, the output signal is given by $v_o(t) = 40 \cdot \sin(2\pi 50t)$ and the resistive load is $R_L = 10\ \Omega$. In order to check the robustness of the design the load has been step changed from open circuit to a 5.7 Ω resistive load, the Figure 11 shows the scaled versions of both the measured output voltage and output current in that case. Finally, a full wave rectifier acting as a nonlinear load has been inserted between the parallel inverter system and the resistive load. The scaled versions of both the measured output voltage and output current in closed loop are shown in Figure 12.

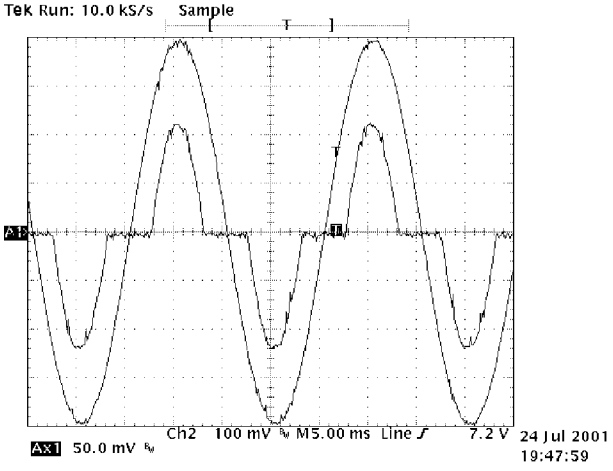

Fig. 12 Measured output voltage and output current of Master-Slave parallel-connected Buck power converters loaded with a full wave rectifier. Voltage scaling factor K = 0.01. Current scaling factor K = 10 mV/A

The total harmonic distortion (THD) has been measured in both cases resulting a 0.2 – 0.3 % in the case of the resistive load and a 0.5 – 0.6 % when the system is loaded with the full wave rectifier.

6. CONCLUSIONS

In this work, a master-slave control scheme based on sliding-mode control technique has been applied to the design of a modular inverter system composed by *N* parallel-connected Buck-based inverters. As a result, output voltage regulation and balanced current sharing among the single inverters is achieved. On the other hand, the overall inverter system sliding domain has been derived in terms of the transfer function of each converter output filter. Accordingly, in the case of resistive loads, a set of design restrictions has been established by means the output filter Bode diagram of each converter and the output signal parameters (amplitude and frequency), this facilitating the subsequent design procedure. Additionally, since the method is general, the sliding domain has been also derived when the inverter system is loaded with reactive or nonlinear loads. Furthermore, this analysis has been applied to investigate whether the steady-state behavior in terms of the output voltage can also be reached when some inverters are added or removed from the modular inverter system. The design has been validated through both simulation and experimental results.

REFERENCES

[1] D. Biel, E. Fossas, F. Guinjoan, R. Ramos, **Sliding Mode Control of a Buck Converter for AC signal generation.** Proceedings of ISCAS'98. Monterey 1998.

[2] D. Biel, E. Fossas, F. Guinjoan, R. Ramos, **Sliding Mode Control of a Boost-Buck Converter for AC signal tracking task.** Proceedings of ISCAS'99. Orlando 1999. pp. 242–245.

[3] E. Fossas, D. Biel, **A Sliding Mode Approach to Robust Generation on dc-to-dc Converters.** Conf. on Dec. and Control. Kobe, Japan. 1996. pp. 4010–4012.

[4] H. Sira-Ramirez, **Sliding Motions in Bilinear Switched Networks.** IEEE Trans. on Circuits and Systems. V. cas 34 N. August 1987. pp. 919–933.

[5] V. I. Utkin, **Sliding Mode and their Applications in Variable Structure Systems.** Mir. Moscow, 1978.

[6] R. Venkataramanan, A. Sabanovic, S. Cuk, **Sliding Mode Control of DC-to-DC Converters.** Proceedings IECON 1985. pp. 251–258.

[7] M. Carpita, M. Marchesioni, M. Oberti, L. Puguisi, **Power Conditioning System Using Sliding Mode Control.** Proceedings PESC 1988. pp. 623–633.

[8] S. Luo, Z. Ye, R. Lin, F. Lee, **A Classification and Evaluation of Paralleling Methods for Power Supply Modules.** Proceedings PESC 1999.

[9] Y. Panov, J. Rajagopalan, F. C. Lee. **Analysis and Design of N Paralleled Dc-DC Converters with Master-Slave Current--Sharing Control.** Proceedings APEC 1997. pp. 436–442.

[10] P. Donoso-Garcia, P. Cortizo, B. R. de Menezes, M. A. Severo Mendes, **Sliding Mode Control for Current Distribution in DC-to-DC Conected in Parallel.** Proceedings PESC 1996. pp. 1513–1518.

[11] H. Bühler, **Réglage par mode de glissement.** Presses Polytechniques Romandes, 1986.

[12] B. Nicolas, M. Fadel, Y. y Chéron, **Sliding Mode Control of DC-to-DC Converters with Input Filter Based on the Lyapunov-Function Approach.** Proceedings of European Power Electronics Conference (EPE) 1995, pp. 1338–1343.

Kaskadno upravljanje paralelno spojenim izmjenjivačima zasnovamo na kliznim režimima. U ovom se članku opisuje postupak projektiranja sustava upravljanja modularnim izmjenjivačkim sustavom sačinjenim od *N* paralelno spojenih izmjenjivača. Sustav upravljanja osigurava regulaciju izlaznog izmjeničnog napona i ravnomjerno strujno opterećenje svih izmjenivača, što se postiže pomoću skupa kliznih površina i odgovarajućeg upravljanja koje osigurava gibanje sustava po njima. Postupak projektiranja sustava upravljanja dodatno je pojednostavljen postavljanjem skupa ograničenja u vidu ograničenja parametara invertera te ograničenja amplitude i frekvencije izlaznog napona. Funkcionalnost sustava upravljanja ilustrirana je simulacijskim i eksperimentalnim rezultatima dobivenim uz otporno i nelinearno opterećenje izmjenivačkog sustava.

Ključne riječi: izmjenjivač, kaskadno upravljanje, paralelni moduli, klizni režimi

AUTHORS' ADDRESSES:

Rafael Ramos
Domingo Biel
Dpt. d'Enginyeria Electrónica. E.U.P.V.G. UPC. C/ Víctor Balaguer s/n. 08800- Vilanova i la Geltrú (Barcelona, SPAIN)
e-mail: {lara, biel}@eel.upc.es

Francesc Guinjoan
Dpt. d'Enginyeria Electrónica. UPC.Modul C4.Campus Nord. C/Gran Capitán s/n. 08034-Barcelona, SPAIN
e-mail: guinjoan@eel.upc.es

Enric Fossas
Institut d'Organització i Control de Sistemes Industrials.
Av. Diagonal, 647, planta 11. ETSEIB. UPC. 08028-Barcelona, SPAIN
e-mail: fossas@ioc.upc.es

Received: 2001–10–05